SEPTEMBER 29, 1982

A CAHNERS PUBLICATION

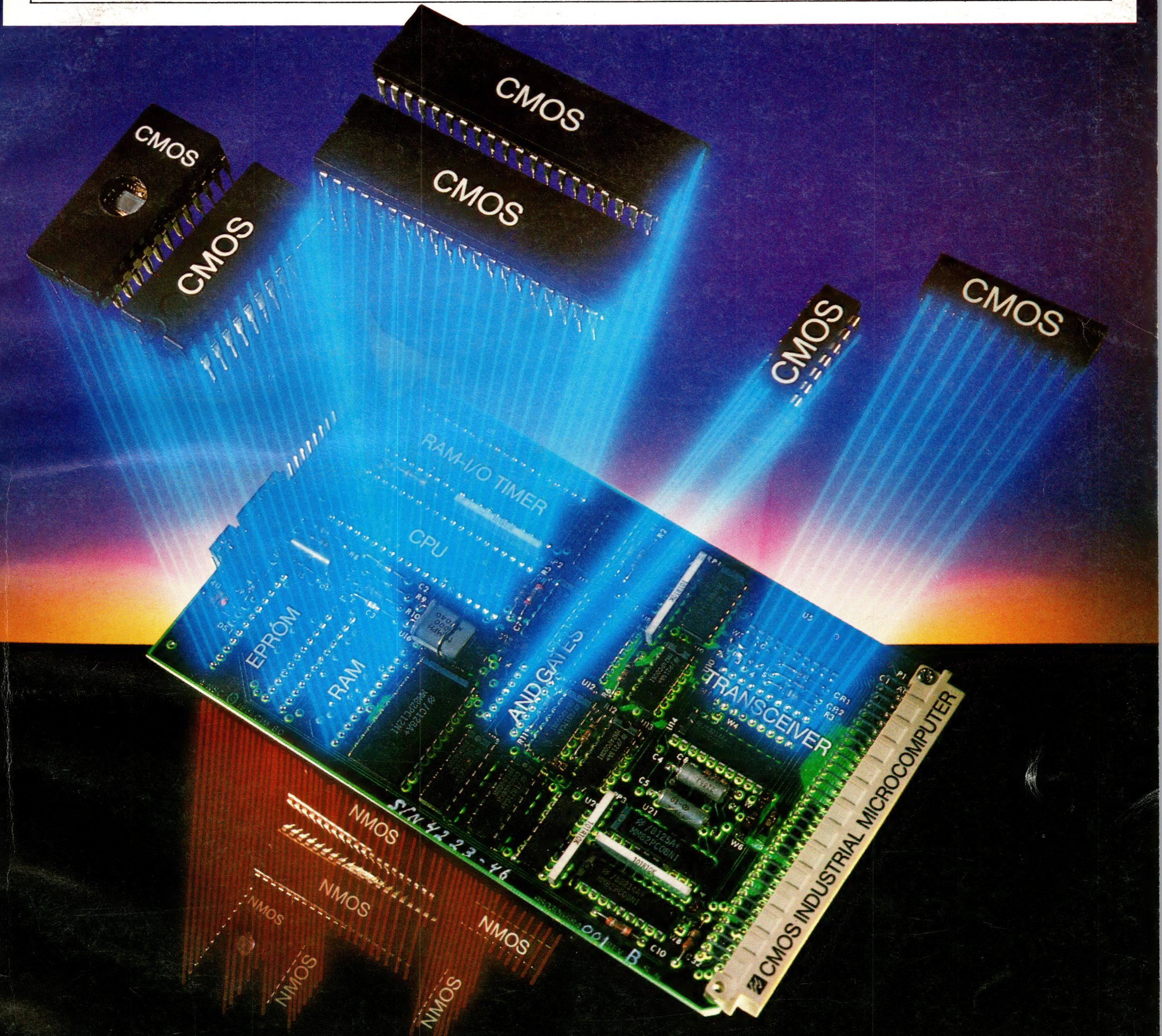
EDN

EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

Consider sensor tradeoffs when designing digital thermometers

Use analog techniques in process control

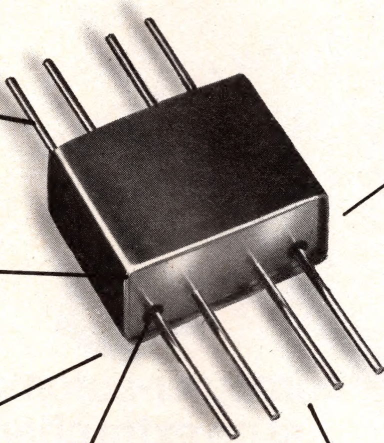
Applications grow for thermal imaging



CMOS technology leaves NMOS behind in increasing numbers of μP/μC designs

tough flatpack mixers

...innovated by Mini-Circuits for rugged applications



Rugged Pins
heavier 25 mil. dia. leads resists wire breakage

Guaranteed for hermeticity
every unit must pass MIL-STD 202 test method 112B condition A and C

withstands wave soldering punishment
reliable pc board assembly eliminates open circuits common with conventional flatpacks. Every unit subjected to thermal shock testing MIL-STD 202 method 107

stronger glass seals
prevents cracking when leads are bent and handled.

tough competitive pricing
only $14.95 (6-24)
½ to ⅕ the cost of conventional flatpacks

Model LMX-113 Superior Electrical Characteristics

FREQUENCY RANGE, (MHz)

LO, RF	5-1000	
IF	DC-1000	

CONVERSION LOSS, dB	TYP.	MAX.
one octave from band edge	6.2	7.0
total range	7.0	8.0

ISOLATION, dB		TYP.	MIN.
5-50 MHz	LO-RF	50	45
	LO-IF	45	40
50-500 MHz	LO-RF	40	30
	LO-IF	35	25
500-1000 MHz	LO-RF	30	20
	LO-IF	25	17

SIGNAL 1dB Compression Level
0dBm min

finding new ways...
setting higher standards

Mini-Circuits

A Division of Scientific Components Corporation
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CIRCLE NO 2

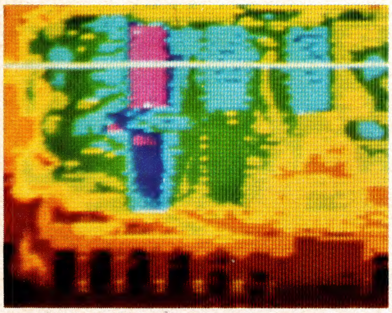
EDN

SEPTEMBER 29, 1982 • VOLUME 27, NUMBER 19 • EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

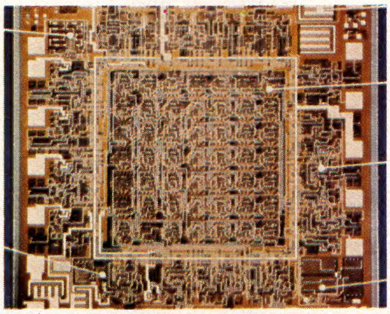
DESIGN FEATURES

TECHNOLOGY UPDATE

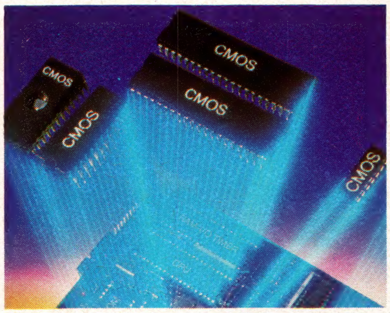
Contents continued on pg 7



Thermal imaging, *long used as a production testing technique, is finding increasing use for many systems as a capable design and prototyping tool as well (pg 41).*



Uncommitted-component arrays *contain transistors, capacitors and resistors plus support functions and encompass four families. Maximum clock rate spans 250 kHz to 10 MHz (pg 75).*



On the cover: *Variants of classical CMOS technology are skyrocketing into system-design use. How do they check out? See pg 88. (Photo courtesy National Semiconductor Corp)*

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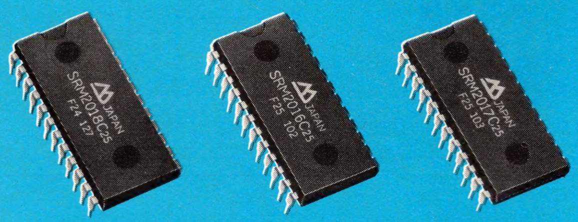
SUWA SEIKOSHA

16K CMOS Static RAM



Epson presents its latest series of CMOS memories for advanced-technology applications.

Model	Org.	Access time (max.)	Standby current (max.)	Availability
SRM2016C20 SRM2016C25	2K×8	200 ns 250 ns	100μA	End '82 Now
SRM2017C20 SRM2017C25	2K×8	200 ns 250 ns	100μA	End '82 Now
SRM2018C20 SRM2018C25	2K×8	200 ns 250 ns	100μA	End '82 Now

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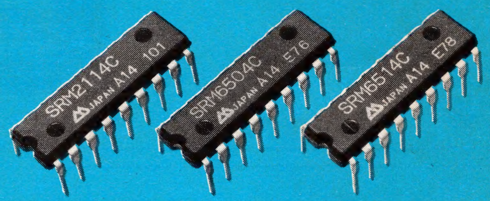
EPSON AMERICA, INC.

3415 Kashiwa Street • Torrance, CA 90505
Telephone (213) 534-0360 • Telex 182412

CIRCLE NO 226

SUWA SEIKOSHA

4K CMOS Static RAM



Epson offers this series of proven CMOS memories which feature high reliability and low power consumption.

Model	Org.	Access time (max.)	Stand by current (max.)	Supply V
SRM2114C3 SRM2114CL9	1K×4	250 ns 1000 ns	5μA 5μA	5 3-5
SRM6504C3	4K×1	250 ns	40μA	5
SRM6514C3	1K×4	250 ns	40μA	5

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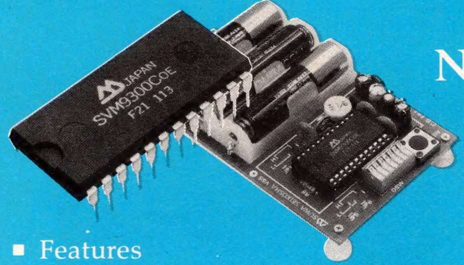
CIRCLE NO 227

SUWA SEIKOSHA

Voice Synthesizer SVM9300 One-Chip CMOS LSI



NEW

- Features
  - • Up to 4 sec. duration time and 6 bit word selecter input • Male voice, female voice, sound effects and imitation sounds • Low power consumption • Low Cost • Built-in voice data mask ROM, DAC, preamplifier and oscillator • 3–5V single power supply • Sound-element synthesizer system
- Applications
  - • Games/Toys • Hand-held battery-driven products
- Evaluation Kit available (chip and board)

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EPSON AMERICA, INC.

Semiconductor Marketing

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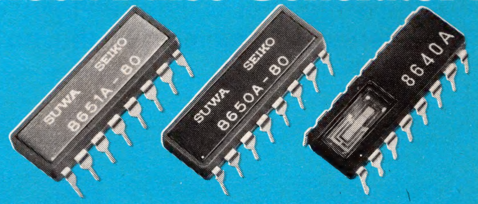
CIRCLE NO 228

Programmable Clock Pulse Generator IC



EVERY IC CAN GENERATE 64 FREQUENCIES

By setting 6 program leads, every 8600 series IC can generate 64 (57 unique) frequencies from the original frequency of its built-in crystal oscillator. Programming is through a 1/1 ~ 1/12 × 10^{-7} C-MOS divider. Power consumption is less than 0.5 mA, and 5V for TTL is provided. Custom original frequencies are available.

Ten SUWA SEIKOSHA ICs Available

Model	Output Frequencies	Output Pulse Frequency Accuracy
8640 A	600 KHz ~ 0.005 Hz	± 100ppm
8640 B	1 MHz ~ 0.0083 Hz	± 100ppm
8640 C	768 KHz ~ 0.0064 Hz	± 100ppm
8650 O	Dividing IC only	
8640 P	Output frequency 50, 60 Hz only	± 100ppm
8650 A	60 KHz ~ 0.0005 Hz	± 50ppm
8650 B	100 KHz ~ 0.00083 Hz	± 50ppm
8650 C	96 KHz ~ 0.0008 Hz	± 50ppm
8651 A	60 KHz ~ 0.0005 Hz	± 5ppm
8651 B	100 KHz ~ 0.00083 Hz	± 5ppm

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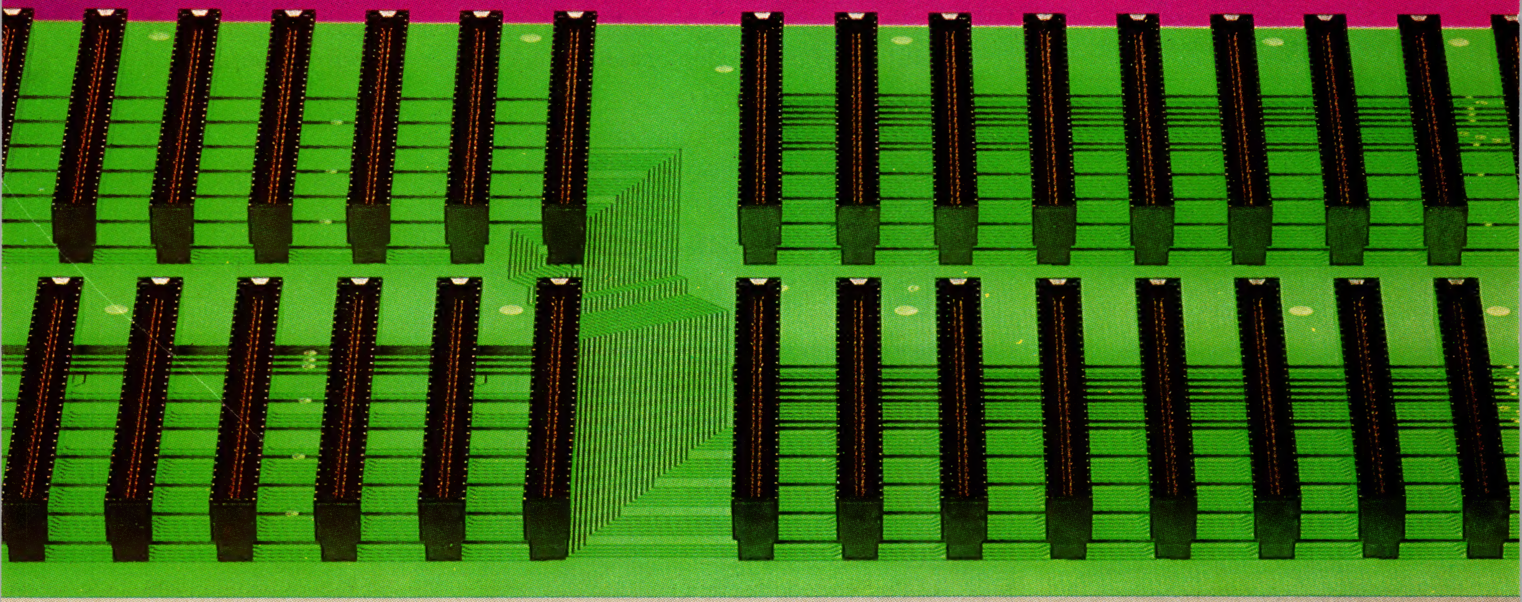
CIRCLE NO 229

EDN SEPTEMBER 29, 1982

Continued from pg 5

WHEN YOUR BACKPLANE DESIGN BALANCES ON A CARD-EDGE, MAKE IT A KE II.

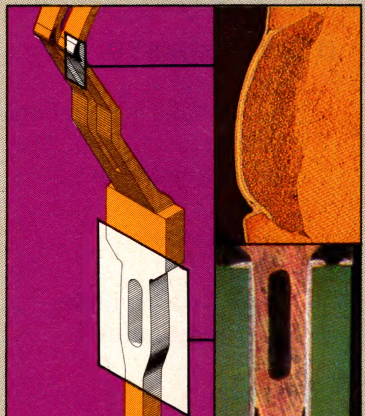


There *is* a low-cost card-edge backplane system that meets the performance demands of high-speed logic forms like ECL and Schottky TTL. KE II.

With the capability for controlled impedance, high current, multiple voltages, noise shielding, and low insertion force. Plus the long-term reliability and easy field replacement of Teradyne's Dynamic Retention* compliant contact.

The world's best press-fit design.

Our compliant, press-fit Dynamic Retention contact ensures a gas-tight interface with the plated-through hole, regardless of the number of layers in the PC panel. Even after all the temperature cycling, humidity variations, and corrosive atmospheres you can throw at it.



At right, a cross section of the Tri-Metal Inlay in the KE II contact mating area. 100 microinches (min.) of gold over nickel and CA725 is welded and mechanically fused into the CA725 contact to form a gas-tight embedment. Note: The inlay is shown overplated with copper for accurate definition of the gold surface.

Bottom, the Dynamic Retention* compliant press-fit contact ensures a gas-tight interface with the plated-through hole, regardless of the number of layers in the PC panel.

*Patent No. RE29513: Designed and developed by Teradyne, Dynamic Retention is the industry's most popular press-fit compliant contact design.

And it's a snap to replace a KE II Dynamic Retention contact. Even in the field. With no risk of damage from soldering, or loss of reliability after repeated replacement.

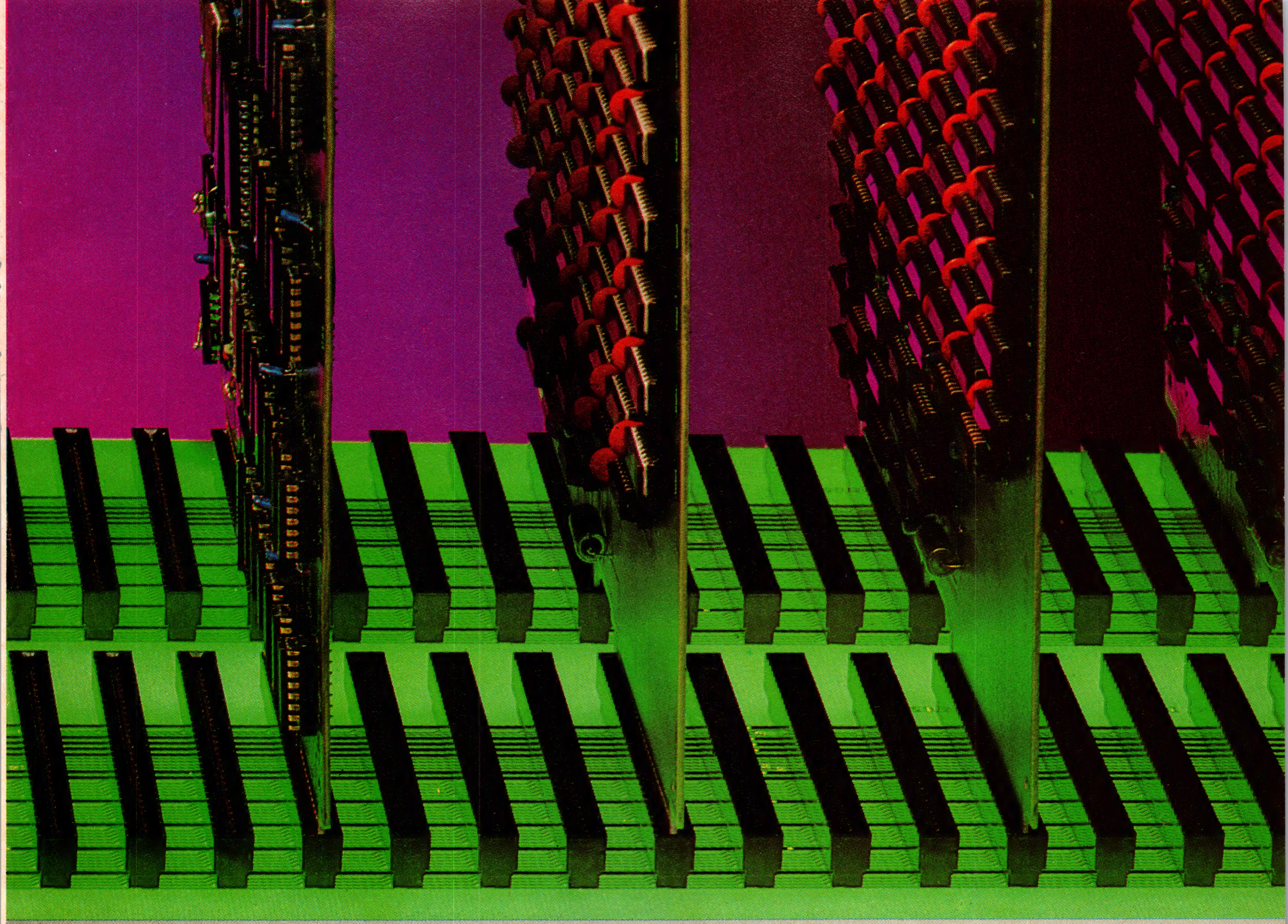
More gold for less money.

Examine the mating surface of the KE II contact. Here, we embed our remarkable Tri-Metal Inlay, successive layers of gold, nickel, and CA725. Thereby placing a minimum of 100 microinches of gold precisely in the critical mating area. And nowhere else.

So efficient is our use of gold, that no surcharge is passed on to you. Which makes KE II backplane systems even more cost-effective.

The contact which holds the inlay deserves close inspection, too. Its geometry delivers the lowest possible engagement force, typically below 5 ounces, without loss of normal force. Which is increasingly important with high-density logic demanding more and more connections.

Naturally, KE II provides a wide variety of grid

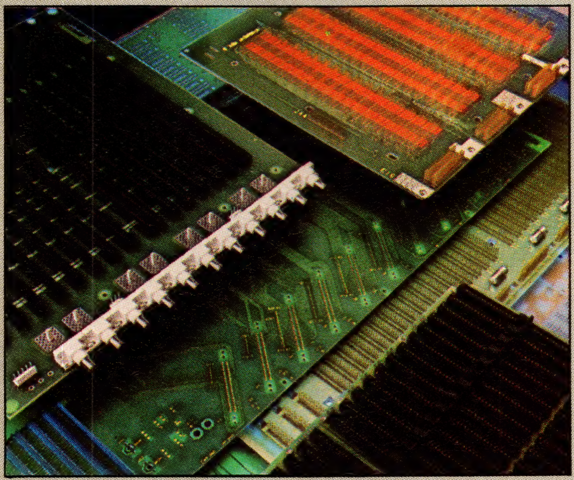


spacings (0.100″ × 0.200″, 0.125″ × 0.125″, and 0.125″ × 0.250″) with insulator slot depths of 0.300″ and 0.350″.

PC panels from the world's foremost facility.

Whether you need double-sided or multi-layer for fully integrated signal and voltage levels. Or copper layers up to 0.060″ thick precisely located within the PC panel for high current-carrying capacity and critical impedance control. KE II is for you.

Because KE II is manufactured in a plant that's designed to handle even your toughest backplane requirements. From heavy copper and tight spacing, to power distribution and multi-layer, our PC professionals offer proven ability in engineer-to-engineer technical assistance, especially during the all-important design stage of your backplanes. And our production capacity can meet your needs many times over.



Whatever the challenge — multi-layer, heavy copper, controlled impedance, power distribution, special testing — Teradyne's proven ability to provide engineer-to-engineer technical assistance during the design stage makes even the most complex backplane system cost-effective.

In summation, the new generation of ICs creates performance demands that only a new generation of card-edge backplane systems can handle.

Only KE II. Only from Teradyne.

We ship more backplanes *on time* than anyone else in the world.

Make Teradyne your design partner. For more information write Teradyne Connection Systems, 44 Simon Street, Nashua, NH 03060. Or call (603) 889-5156.

TERADYNE

CIRCLE NO 4

"The new Fujitsu Microelectronics 64K CMOS EPROM is ideal for my unique, low-power application."

The first 64K CMOS EPROM!

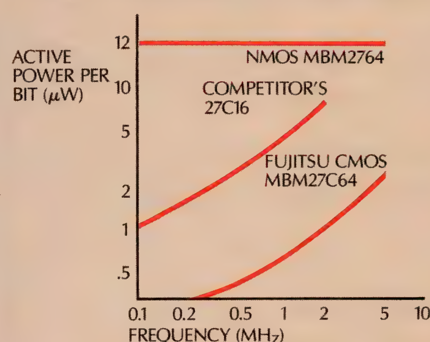
The 64K CMOS EPROM from Fujitsu Microelectronics is here, and it's everything you could want in an EPROM—low power, high speed, extended temperature range, and 8K bytes!

EPROM Comparison Chart—MBM27C64

DEVICE TYPE	ACCESS TIME	POWER PER BIT		SUPPLY CURRENT	
	(MAX)	ACTIVE	STANDBY	ACTIVE	STANDBY
Fujitsu MBM27C64 64K-BIT CMOS**	250nsec	2.4μW	8.0nW	30mA MAX	100μA MAX
Competitor's 27C16 16K-BIT CMOS	450nsec	8.0μW	32.0nW	25mA MAX	100μA MAX
Fujitsu MBM2764 64K-BIT NMOS	200nsec	12.0μW	2800nW	150mA MAX	35mA MAX

** 200nsec PART AVAILABLE SOON

Active Power Per Bit vs. Operating Frequency



To make your compact, portable design really fly, contact your Fujitsu Microelectronics sales office listed below and ask for the Introductory Data Package.

FUJITSU MICROELECTRONICS

FUJITSU MICROELECTRONICS SALES OFFICES:
Boston 617/964-7080; **Chicago** 312/934-6400; **Dallas** 214/669-1616; **New York** 516/273-6660; **Northern California** 408/866-5600; **Southern California** 714/547-9525.

Creating New Horizons... in EPROMs.

CIRCLE NO 5

Hewlett-Packard on Computer-Aided Engineering

Solving sophisticated design calls for a lot of software. But the you have to write it.

To make the best use of your engineering skills, you need to be free from doing lots of routine, time-consuming calculations. And free from having to re-invent the wheel each time you tackle a specific problem.

That's why at HP, we're building a library of affordable software solutions for engineers. With over 50 EE packages already available, it's a good bet we have one that closely matches your needs. From PC board design to circuit simulation to waveform analysis. And that means a running head start on getting your product to market.

A faster way around the circuit.

Our new Engineering Graphics System (EGS/45), for example, can help you create printed circuit board artwork, electronic schematics, general engineering drawings and tooling output to numeric control equipment. In as little as half the time it would take manually. And because all "drawing" is done with easily manipulated symbols on the CRT, you'll do it with increased accuracy, better quality and more flexibility.

Getting your design completed faster is also the idea behind our new HPSPICE circuit simulation software. With HPSPICE, you can quickly simulate, analyze and verify the

problems
re's no reason

operation of electronic circuits, and graph the output on one of our HP graphics peripherals. The result is less time spent in the breadboard and debugging stage, and more time on important design tasks.

The list goes on. Including a Statistical Analysis Pac that combines software programs for statistics, data manipulation and regression analysis into one integrated package. And an Electronics Engineering Pac that contains programs for A.C. circuit analysis, waveform analysis and math.

Part of a bigger story.

There are engineering solutions available to run on a wide range of HP systems, from personal computers to desktops to our larger HP 1000 systems. Our software packages are also part of HP's Manufacturers' Productivity Network (MPN), a step-by-step approach to linked computer solutions throughout your company.

In addition, many programs are available from third parties under our HP PLUS program, in which we work with software suppliers to bring competitively priced, quality solutions to the marketplace.

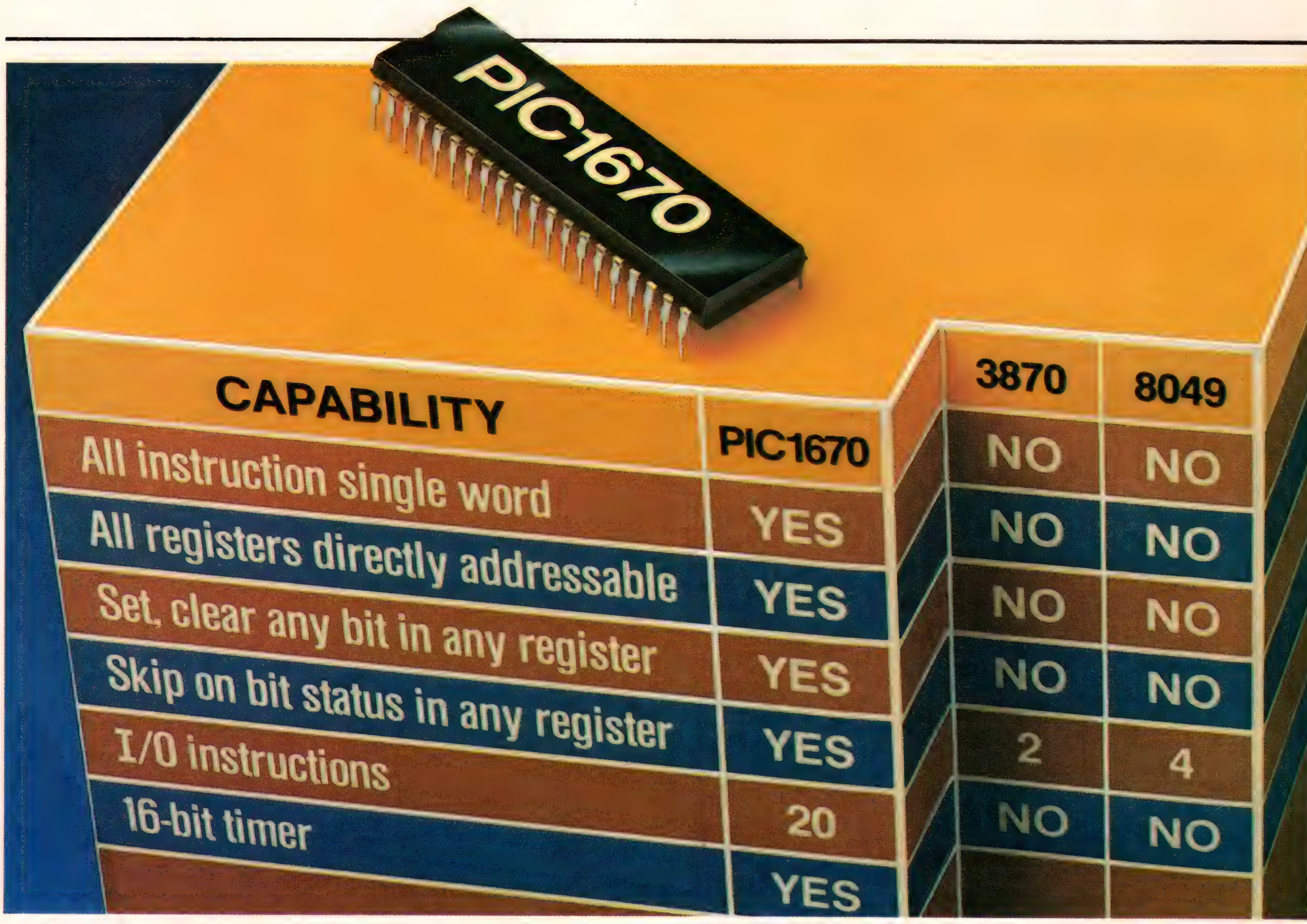
To find out more about our software and hardware products for electrical engineers (including any of the titles you see here), contact your local HP sales office listed in the White Pages. Or, write for more information to Hewlett-Packard, Attn: Franz Nawratil, Dept. 20132, 11000 Wolfe Road, Cupertino, CA 95014.

HEWLETT PACKARD

CIRCLE NO 6

TCG201
HPTC-60

The New PIC1670 Microcomputer. The Obvious Choice.



Compare the new PIC1670 microcomputer to the competition and see for yourself how its unique architecture provides superior performance and cost-effectiveness.

As the comparison chart plainly shows, the new generation PIC™ microcomputer—the architecturally advanced PIC1670—is clearly ahead of the competition in virtually every category. Yet for all its high performance and proven efficiency, you don't pay a higher price. You do get a microcomputer that meets the demands of your most challenging designs, fast prototype turnaround, and on-time delivery.

The architectural advantage that's the hallmark of all PIC microcomputers, gives the new PIC1670 more efficient bit handling capability. It can test and skip on bit status, rather than rely on the masking technique of coventional microcomputers. In addition, the PIC1670's innovative 13-bit instruction word gives it superior performance compared with conventional 8-bit microcomputers, and it uses far less ROM for significant cost savings.

Also new to the PIC family is the PIC16C55 low power CMOS microcomputer which operates over a wide voltage range of 2.5 to 6V and draws only 2mA. And remember, while these devices are the latest generation of PIC microcomputers, they are by no means the last.

To learn more about the PIC microcomputer family call the General Instrument Microelectronics office nearest you.

We help you compete.®

GENERAL INSTRUMENT

Sales Offices USA: CA, 213-322-7745 or 408-496-0844; **FL,** 813-577-4024; **IL,** 312-981-0040; **IN,** 317-872-7740 or 219-291-0585; **MI,** 313-391-4070; **MD,** 301-269-6250; **NC,** 919-876-7380; **NH,** 603-424-3303; **NY,** 516-733-3107; **PA,** 215-643-5326; **TX,** 214-934-1654; **EUROPE: Frankfurt,** (6103) 23 051; **London,** 01-439-1895; **Milano,** (02) 720914; **Munchen,** (089) 27 24 049; **Paris,** (1) 365 72 50; **Stockholm,** (08) 679925; **ASIA: Hong Kong,** (5) 434360; **Taipei,** (02) 914-6234; **Tokyo,** (03) 473-0281

CIRCLE NO 7

News Breaks

Edited by Joan Morrow

CAD SYSTEM SUPPORTS IC DESIGN, FABRICATION

A complete single-user chip-layout system, a symbolic gate-array design package and a fabrication agreement with Master Logic (Sunnyvale, CA) combine to provide what VIA Systems Inc (Billerica, MA) terms cradle-to-grave IC-development support. The firm's CAD system supports fully custom IC-design functions as well as manual gate-array placement and routing, using a function library and a 5-μm ISO-CMOS chip design developed by Master Logic. VIA's $90,000 LSI-11/23-based Model 110 workstation features a 640 × 512-pixel color-graphics display, a 35M-byte Winchester disk drive, a 17M-byte cartridge tape drive, on-line design-rule-checking software and a data tablet. The $140,000 Model 130 system adds an 800/1600-bpi, 75-ips tape drive plus pattern-generation; Applicon-, Calma- or MANN-9400-interface; and macroprogramming software. Both systems run RSX-11-based software (operating system not included) and thus accommodate a range of applications software.

Using VIA's GATES (Gate-Array Technology and Engineering Support) software, you can design 50-, 200- and 400-gate circuits compatible with specially designed Master Logic chips. The arrays' constant-width routing channels and highly regular cell structure facilitate manual interconnection design using a preprogrammed function library. You can purchase chips directly from Master Logic or order prototypes through VIA; Master Logic offers design-support services for array users, and VIA offers applications-support contracts and cell-library update subscriptions.—Andy Rappaport

LARGER SCOPE SCREENS EASE VIEWING, MEASUREMENTS

Incorporating 9.5 × 12-cm graticules to simplify readings, Hewlett-Packard's (Palo Alto, CA) Models 1745A ($2840) and 1746A ($3140) achieve the measurement accuracy of the firm's 100-MHz 1740A, which uses an 8 × 10 graticule. The more than 40% increase in screen size improves visual resolution, especially in calculations such as rise time, while an antireflective coating provides a sharp trace without annoying reflections. A third-channel trigger-view feature on both units lets you display the trigger signal along with the two vertical channels. Finally, when you combine the 1746A's dual-marker delta-time system with an optional DMM, you can read out time intervals with accuracy near ±0.5%.—Paul G Schreier

LOW-COST KIT HELPS EVALUATE 5¼-IN. HARD-DISK DRIVES

Offering a fast and inexpensive opportunity to check out its 5¼-in. SA600 hard-disk drives, Shugart Associates (Sunnyvale, CA) furnishes an evaluation kit that contains an SA604 6.66M-byte drive, an SA1410A intelligent controller, cables and documentation. The kit sells for $995 to qualified OEMs through Hamilton/Avnet distributors.—George Kotelly

6800/6809 NETWORKING SOFTWARE TO ALLOW RESOURCE SHARING

Software Dynamics (Anaheim, CA) plans to extend the capability of its SDOS operating system: Beginning in December, you'll be able to add SDNET—a networking software package that will allow multiple processors to share expensive peripherals and dedicated system hardware. SDNET will tie together as many as 255 local computers via a twisted wire pair; data rates will run as high as 125k bps. The software's message protocol resembles Ethernet packets; cost will be approximately $150.—Ed Teja

RUGGEDIZED PORTABLE DMM FEATURES 10A AC/DC RANGES

Suited for use in rough environments, Beckman Instruments's (Brea, CA) $189 Model HD-110 portable DMM meets MIL T-2880 shock and vibration specs and thus can withstand accidental drops. The 3½-digit instrument is waterproof and dustproof and withstands voltage inputs to 1500V dc or 1000V rms and current to 2A/600V. (It safely handles 20A unfused for 30 sec.) Resistance ranges are protected to 600V dc. Peak measurement ranges

include 1500V dc, 1000V ac, 20 MΩ plus 10A ac or dc. The instrument's LCD allows continuous 2000-hr operation from a 9V alkaline battery.—Paul G Schreier

CMOS GATE ARRAYS REQUIRE NO POLYSILICON

Plessey Semiconductor's (Irvine, CA) CLA Series ISO-CMOS gate arrays feature 2-layer metallization and no polysilicon. By allowing intergate connection without using highly resistive polysilicon layers, they provide 3.5-nsec typ NAND-gate delays and worst-case propagation time of 7 nsec with a fanout of 3. In addition, the 2-layer-metallization system permits typical silicon utilization of 85 to 90%. The 5-μm-geometry array series comprises three versions: CLA-2500 parts include 2400 gates; CLA-2300 arrays, 1440; and CLA-2100 devices, 840. Plessey expects to introduce 2000- and 500-gate versions late this year.

To facilitate rapid array design, the firm offers an automated design system that supports circuit simulation, computer-aided interconnection routing and test-vector generation. Array prices vary with size, complexity and vendor support required.—Andy Rappaport

MULTITASKING INDUSTRIAL CONTROLLER DOUBLES AS PERSONAL COMPUTER

Consisting of two boxes, each the size of a personal computer, the less-than-$10,000 Macsym 350 from Analog Devices Inc (Norwood, MA) combines the functions of a personal computer with those of an industrial control system. The first unit, a system console, contains an 8086/8087 chip set, 128k bytes of RAM, a graphics controller, dual floppy-disk drives (320k bytes each), a separable keyboard and a black-and-white graphics monitor. The console also provides six slots for memory expansion, an RS-232 or -422 port and IEEE-488 capability. The second box, a measurement front end, ties to the system console over an RS-422 link. It uses an 8088 and 128k bytes of RAM and provides 16 slots for any Macsym-family I/O boards, which allow screw-terminal connection to transducers, sensors and activators. You program the unit in MACBASIC (measurement and control BASIC), and the system handles 18 simultaneous tasks in real time. Because it's CP/M-86 compatible, the system also runs widely used word-processing, spreadsheet and other application packages.—Paul G Schreier

MULTIBUS-COMPATIBLE 1-CARD COMPUTER COMBINES UNIX AND A 68000 μP

Heurikon Corp (Madison, WI) has unveiled its HK68 single-board computer, which furnishes both the 68000 μP and Bell Labs's UNIX operating system. The Multibus-compatible board also provides four serial ports, DMA, a memory-management unit, two iSBX connectors, two ROM sockets and on-board memory space for as much as 1M bytes of RAM. Fully loaded, it costs $3895.—Ed Teja

64K CMOS ROM UPDATES CONTENTS UPON ADDRESS CHANGES

Consuming 50 μA in standby and 5 mA operating, the 8k × 8 HCMP 23C64 static CMOS ROM from Hughes Solid State Div (Newport Beach, CA) updates its output when any address changes. It operates from one 4 to 6.5V supply; at 5V, typical access time equals 350 nsec. The $8.90 (10,000) device comes in 24-pin hermetic ceramic or plastic DIPs.—Paul G Schreier

FOR YOUR CALENDAR . . .

The 1982 Global Telecommunications Conference (formerly the National Telecommunications Conference) is slated for November 29 to December 2 at the Sheraton Bal Harbour Hotel in Miami, FL. At this 4-day conference, the theme "Communications—A Synergistic Technology" will be explored through discussions on local-area networks, fiber optics, mobile radio, satellite communications, computer/communication security, network performance evaluation, teleconferencing, LSI/VLSI communication systems, speech/signal processing and voice/data integration. For more information, contact Dr Liang Li, publicity chairman, Gould SEL, Box 9148, Ft Lauderdale, FL 33310, or phone (305) 587-2900.—Joan Morrow

JAPANESE FIRMS PLAN TO EXPORT 16-BIT PERSONAL COMPUTERS TO USA

Several major Japanese electronics firms that are concentrating their domestic efforts in the low end of the personal-computer market will be competing soon with US makers of 16-bit personal computers. Expect Mitsubishi, Sord and Toshiba to export systems before the end of this year; Matsushita, Hitachi and Sanyo should bring their 16-bit computers to the US by next April. Most of these Japanese systems should be software compatible with the IBM Personal Computer.—Joan Morrow

JAPANESE CAD/CAM PC-BOARD SOFTWARE TO MAKE USA DEBUT

Hewlett-Packard and Zuken Shori-Gijutsu Kenkyusho (Yokohama) have signed an agreement that allows the Palo Alto, CA firm to market Zuken's CAD/CAM software in Europe and North America. Zuken unveiled the System 2000 package at the Auto Fact 4 CAD/CAM show in Philadelphia this month and expects to ship $3 million worth of the software in 1 yr.—Joan Morrow

FIRM PLANS GATE-ARRAY EXPORTS, INTROS 64k DYNAMIC RAM

Mitsubishi Electric Corp will supply an estimated 1000 gate arrays to IPL Systems of Massachusetts. IPL should use the gate arrays in an IBM plug-compatible machine that will compete with IBM's 4300 Series.

Separately, Mitsubishi has developed a 64k dynamic RAM featuring 100-nsec access time. Four versions of the device, which uses one 5V power supply, sell for 3500 yen ($14) in plastic; $16.80 in ceramic.—Joan Morrow

JAPANESE SEMICONDUCTOR FIRMS INCREASE CAPITAL INVESTMENTS

Because of the worldwide shortage and demand for 64k RAMs, Nippon Electric, Fujitsu Ltd and Toshiba Corp have re-evaluated their investment programs for fiscal 1982. NEC has put another $16.7 million into its production of 64k dynamic RAMs and microcomputer chips. Toshiba has added $41.7 million from its original $108 million investment and Fujitsu plans to spend a total of $172 million in semiconductor production during this fiscal year.—Joan Morrow

VLSI MEMORY TESTER SIMULTANEOUSLY EXAMINES FOUR DEVICES

The DIC-8020B/E from Ando Electric Co simultaneously tests four memories when used with the firm's parallel automatic handler. The 30 million yen ($120,000) 20-MHz system features a 64-bit × 256-word microprogram memory that allows generation of complex test patterns without a dummy cycle. By keying in the monitor command, a user can collect evaluation data without altering the test program during line test. Although the system is designed for 64k dynamic RAMs, it can also accommodate 256k dynamic RAMs or large-capacity static RAMs or ROMs.—Joan Morrow

HITACHI, NEC TO ESTABLISH US DESIGN CENTERS

Hitachi Ltd is expected to set up a US base for the design and development of microcomputer chips. Tentatively named Application Laboratories, the center will employ American software-development engineers.

Nippon Electric Co will also establish a US software-development center for microcomputer chips. This new company will originally be organized as part of NEC Electronics USA but later become an independent firm that will also accommodate the software needs of the parent company in Japan. Nippon also plans to hire US software engineers.—Joan Morrow

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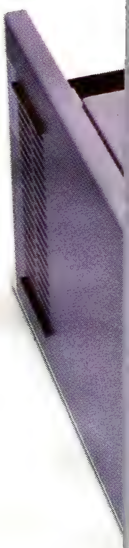

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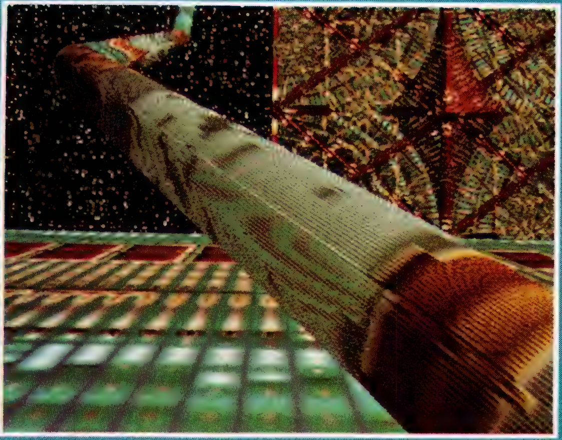
The editors of EDN are proud to offer a limited edition of three works of computer generated art by David Em.

These prints showcased in the October 14 EDN special section **Electronic Technology: The Next 25 Years** are each 20″ x 26″ and have been printed on high quality presses.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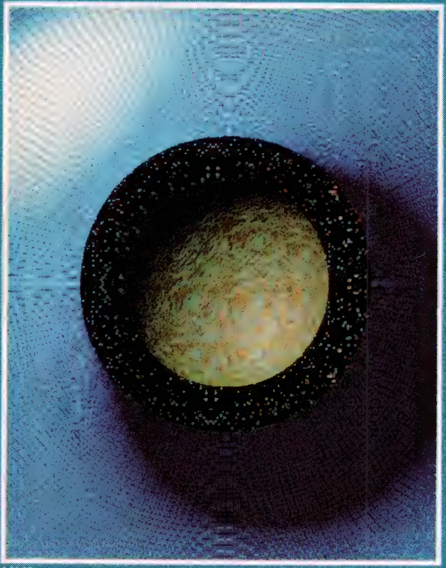
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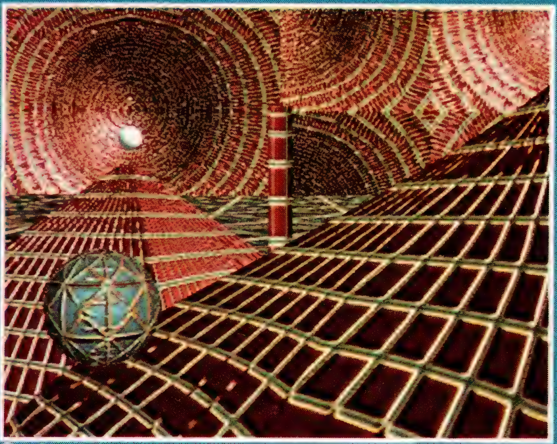
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Editorial

A golden opportunity to standardize

As the Dept of Defense (DoD) pins down its specification for ADA, commercial activity in that programming language has begun to explode. The mere promise that almost all DoD programs will eventually have to be written in ADA has prompted many vendors to jump on the bandwagon. In fact, several partial implementations of ADA compilers are commercially available—for mainframes, minis and even personal computers.

ADA's unique features should change the commercial programming landscape, especially for large design projects. Of the language's many features designed to improve program reliability and productivity are packages that allow for the definition of abstract data types and the enforcement of ADA's rich semantics across compilation units. These units permit you to separately compile the overall program structure and thereby force all design-team members to adhere to the structure's requirements, greatly reducing interfacing problems and allowing you to isolate and identify whose code is causing problems.

ADA also promises total portability. DoD intends to require that any ADA program compile on any ADA translator, albeit with varying speed and efficiency. In fact, it has begun to contract with software vendors to write ADA application packages without specifying the target hardware. A whole new cottage industry of ADA-package suppliers will likely arise, and when it does, system designers will be able to select subprograms and merely write "glue code" to implement an application.

The state of the art is closer to this reality than you might think. As noted, partial ADA compilers are already available, and Intel is just announcing its compiler, which is basically the DoD ADA reference manual (the proposed standard), with three pages of exceptions and 11 pages of extensions. (The exceptions deal primarily with aspects of the spec that aren't completely defined and will be eliminated before Intel obtains DoD approval; the extensions consist of instructions that use unique features of Intel's target machine, the 432.)

Although Intel's offering is perhaps the closest thing to a full ADA now on the market, its modifications hold great significance: They might raise compatibility problems.

To ensure true portability, all ADA compilers must be compatible. Recognizing this fact, DoD plans to establish a validation facility and issue the trademarked name ADA only to approved compilers. Exceptions and extensions will reportedly not be tolerated. EDN urges DoD, in defining its validation procedures, to maintain its hard line on this requirement, despite industry pressure for variations such as subsets and despite the fact that a standardized language won't take full advantage of all the hardware on the market—especially object-oriented architectures that are now emerging. Portability's cost benefits to industry will far outweigh any hardware tradeoffs.

Furthermore, DoD should consider permitting software switches in ADA compilers; such switches would disable nonstandard instructions related to specific hardware. Suppliers will want to gain a competitive edge in the commercial marketplace through their unique hardware, and this approach will discourage them from flooding the market with both validated and nonvalidated versions, confusing matters even more. DoD has a unique opportunity to force ADA standardization and should do all in its power not to compromise the effort.

Paul G. Schreier

Paul G Schreier
Editor

An Award-Winning Magazine
1981 *Subject Analysis:
Electronic Technology—The Next 25 Years
1981 *Editorials
1981 **ASBPE Excellence in Writing (3rd place):
Seventh Annual µP/µC Chip Directory
1978 *Staff-Written Series:
System Design Project
1978 *Contributed Series:
Designer's Guide to Fiber Optics
1977 *Contributed Series
Software Design Course
1976 *Special Issue:
Microprocessor Reference Issue
1975 *Staff-Written Series:
Microprocessor Design Series

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Signals & Noise

An error crept in

Dear Editor:

I was pleased to see my Design Idea for the AD594 in the July 16 issue of EDN (pg 427). The editor, however, evidently decided to explain something I hadn't mentioned: that "you can determine the chip's temperature remotely by measuring the total value and subtracting the chip's fixed requirements."

I hadn't mentioned subtracting the chip's current because doing so results in the wrong answer. The important feature of the 2-wire measurement is that the total current, including the chip operating current, passes through the 5.2Ω resistor. As a result, the amplifier adds only enough current to the operating current to make the total loop current equal 10 μA/°C. No subtracting is necessary or wanted.

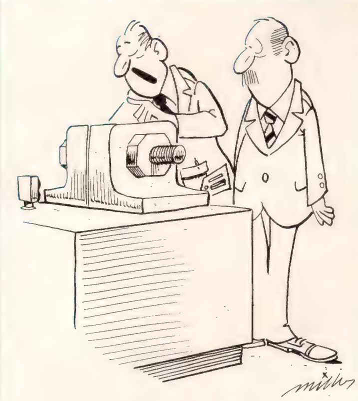
Best regards,

A Paul Brokaw
Division Fellow
Analog Devices
Semiconductor Div
Wilmington, MA

Add two hybrid vendors to manufacturers list

Two vendors were inadvertently omitted from the list in EDN's Special Report on military and high-reliability hybrids (June 23, pg 102). Solitron Devices Inc (1177 Blue Heron Rd, Riviera Beach, FL 33044, phone (305) 287-5000) manufactures custom hybrids and has participated in most major US defense and aerospace programs. And Vitarel Inc (3572 Corporate Ct, San Diego, CA 92123, phone (714) 292-8353)

Continued on pg 37



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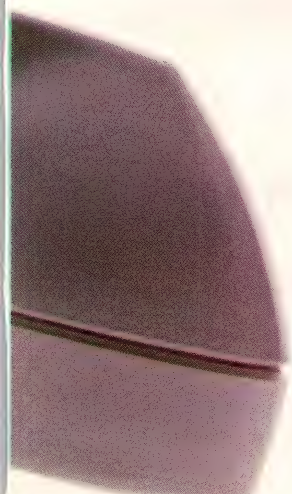
The next way to field program



Spring, 1976. Synertek introduced the first in its family of 6500 8-bit microprocessors.
The rest is history.

1976. 6500 Family gains flexible peripheral control with Synertek's SY6521 peripheral interface controller.

1977. Synertek's single-chip SY6551 UART/baud-rate generator links 6500 microprocessors with serial communication data sets and modems.

1978-1980. Die size is reduced by 30%. Yields increase, prices decline.

1980. Synertek's SY6545 CRT controller provides interface to CRT and raster-scan displays.

1981. Synertek becomes the world's largest producer of 8-bit microprocessors.

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A Z8 that operates at 12-MHz speeds, late in 1982.

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A choice of development tools to fit any budget, starting with our versatile MDT 2000 with Z8 in-circuit emulation.

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cut down on problems caused charge.

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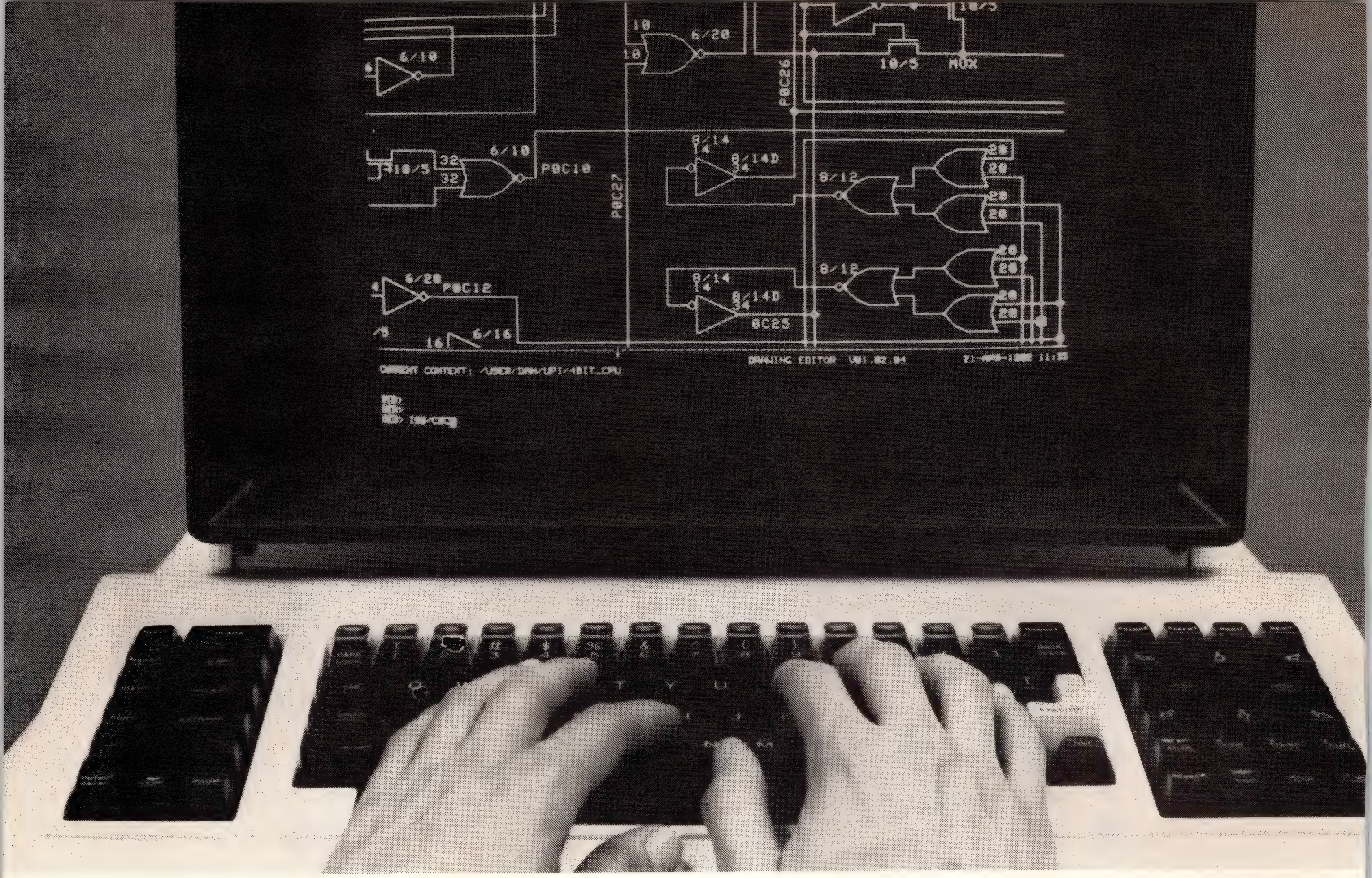

Introducing 8 ways to better electronic design analysis–from an unbeatable combination.

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LOGIS: A general-purpose, 15-state logic simulator with emphasis on MOSFET integrated circuit logic design.

TEGAS: A general-purpose logic simulator for design verification, timing analysis and test generation.

Device Simulation

GEMINI: A MOS device simulator capable of analyzing the operation of a variety of two-dimensional insulated-gate semiconductor device structures.

Manufacturing—Process

SUPREM2: Simulates steps in the integrated circuit manufacturing process. Output consists of all the dopants present in the silicon and silicon dioxide.

Manufacturing—Automatic Device Characterization

MODGEN: Generates ASPEC MOS model parameters from IV and CV data taken from actual devices.

Layout—Design Rule Checking

DRC: A program that verifies that the layout of an integrated circuit conforms with rules specified by the wafer processing facility.

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specializes in military, aerospace and medical-electronics circuits and offers dual-cavity hybrids that include components mounted to both sides of a substrate. EDN regrets the omissions.

Correct a price error

The $11,000 price published for Forward Technology's (Santa Clara, CA) Gateway Scientific Workstation (EDN, July 16, pg 20) covers the 68000 processor, 256k bytes of memory, a 15-in. display, a VT-100-compatible keyboard and a graphics controller. Adding Bell Labs's UNIX operating system, C and FORTRAN 77 compilers, graphics software and a Winchester disk drive brings the cost into the $23,000 range.

Divide by 10

Because of an editing error, **Eq 1** in "Formula simplifies inductance calculation" (EDN, August 4, pg 164) yields solutions 10 times greater than the correct value. To calculate a coil's true inductance, L (not impedance as stated), amend **Eq 1** to read:

$$L=0.070(CN)^2/(1.908C+9.0H+10.0B).$$

In addition, in the Design Idea's example, the coil's thickness, B, was printed incorrectly; the correct value is 0.0342 in.

Your turn...
EDN welcomes your comments, pro or con, on any issues raised in the magazine's articles. Address letters to **Signals and Noise Editor, EDN, 221 Columbus Ave, Boston, MA 02116.** Names will be withheld upon request. We reserve the right to edit letters for space and clarity.

This small digital panel instrument has one big thing going for it.

Technology Update

Sophisticated thermal-imaging systems pinpoint prototype-stage heat problems

Jesse Victor, Senior Staff Editor

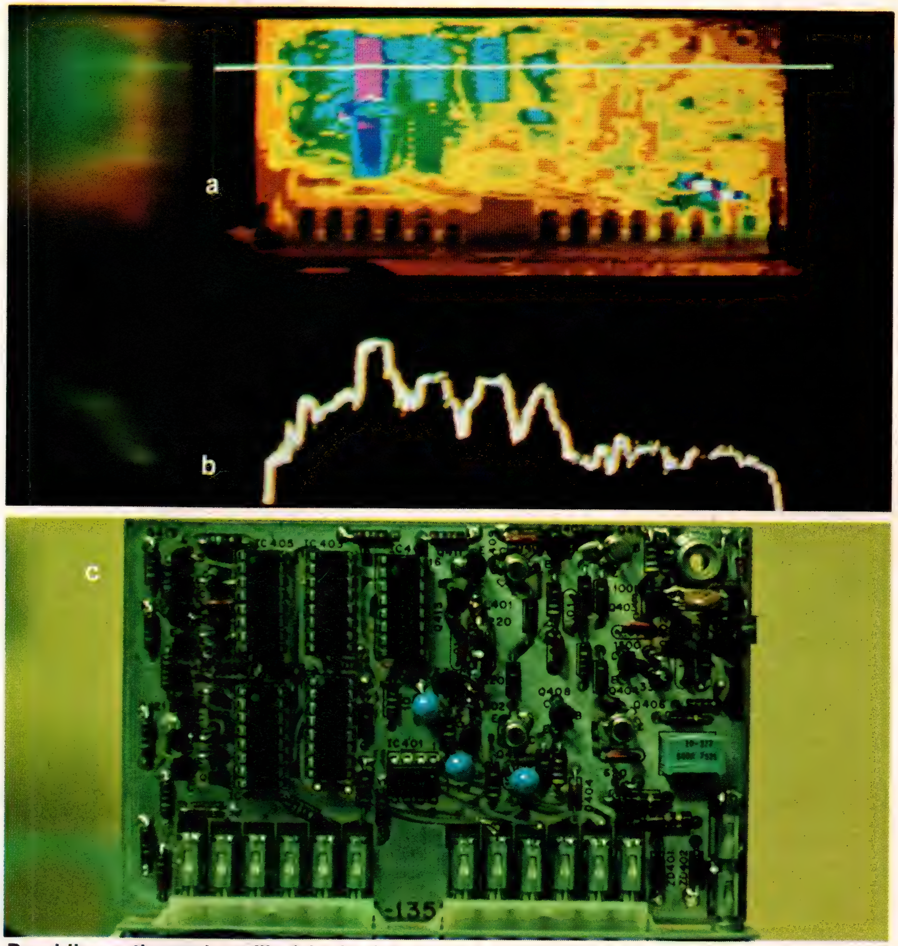
Designers are increasingly using thermal-imaging systems early in the design cycle—in the prototype or model stage—to spot heat-induced problems in electronic assemblies before they cause high board-failure rates in production or subsequent development testing. Replacing traditional hit-and-miss thermocouple-testing techniques, thermography had its genesis in medical applications and has been earning growing credibility as a fast, accurate and versatile tool for both in-house and field testing. With its use spurred by production-test rejection rates as high as 30% and by increasing circuit complexity, it's thus emerging as a significant design technique for improving product reliability.

Reducing temperature problems

Temperature-related problems are one of the major causes of electronic-component failure—by some estimates accounting for 60% of all in-service device failures. And most of these failures are traceable to inadequate or marginal provisions for heat dissipation.

Although new electronic-assembly designs are functionally tested and usually subjected to thermal testing as well, high product-failure rates in many cases result from the failure of conventional thermal-testing techniques, in which thermocouples are applied to locations in which heat buildup is suspected.

Specifically, although conventional thermal testing provides an accurate measure of temperature at the test points, its effectiveness depends entirely on the designer's estimate of where a circuit's critical heat-concentration areas are located. If this estimate is proved wrong



Providing a thermal profile (a) *of a fully loaded pc board* **(c),** *a thermal-imaging system's CRT display also graphs the temperature variations* **(b)** *along the part of the board traversed by a movable horizontal cursor (white line crossing upper portion of board in* **(a)**). *Colors show the gradient from highest (indigo) to lowest (orange-brown) temperature.*

Up from medical imaging

Thermal imaging was originally developed by the medical community as a diagnostic tool for cancer detection. Using infrared scanning to measure the variations in heat emitted by a test subject, it converts the scanned object's surface thermal pattern into a visible image that can be examined and recorded photographically.

During the past decade, thermography has also found wide use in the electronics industry—primarily to identify shorted or open circuits and inoperative components in failed electronic assemblies. Multilayer circuit boards, for example, are now tested using this technique, which can provide a look at inner-layer thermal distribution.

Employed primarily in production-test facilities, thermal-imaging systems are most commonly used to supplement traditional automatic test equipment when the ATE is unable to unambiguously isolate a fault. Thermographic technology, however, is moving one step back in the design process; it's now also used to verify or modify thermal-design assumptions in the breadboard or prototype stage.

by the test itself or by subsequent device failures, new circuit heat-dissipation techniques must be devised and a new round of time-consuming tests performed.

Infrared thermal imaging, however, can avoid this type of trial-and-error analysis. A typical system, such as the UTI Instruments Model 900 used at Lockheed-California Co's Quality Assurance Lab, can scan a prototype assembly in 2 sec, produce a thermal profile of the device under test (**photos**) and provide temperature data that would require the simultaneous application of approximately 300,000 thermocouples (see **box,**

How thermography works

Lockheed-California's Model 900 thermal-imaging system (photos, **(a)**) consists of two major components: an imager assembly and infrared detector that view the test subject and display its thermal image on a CRT, and a digital image-processor/memory system that converts the scan data into the visual image.

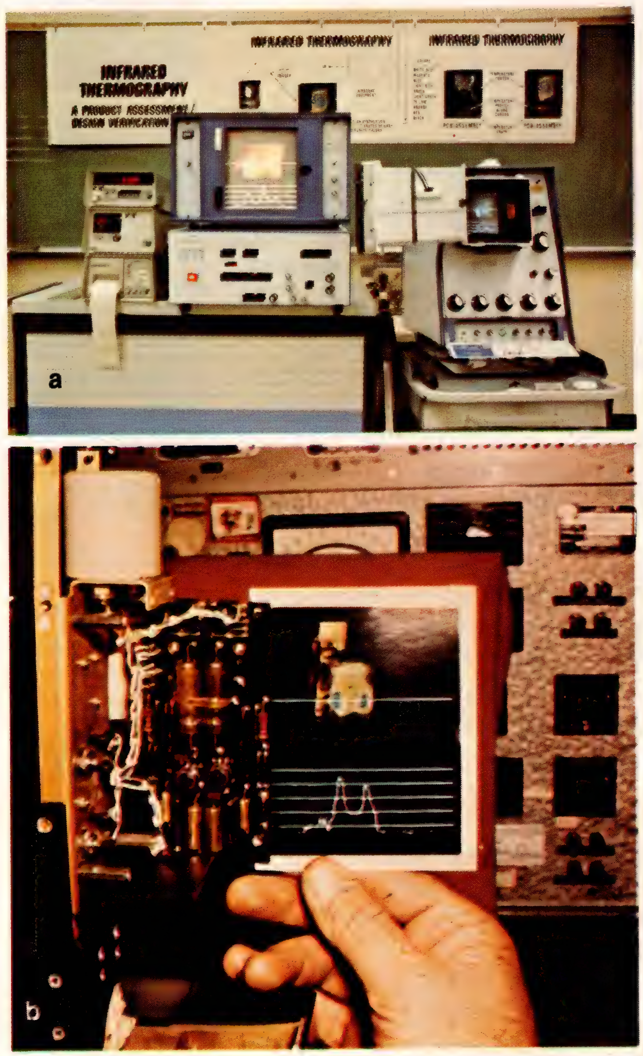
When the thermal imager scans a device under test, a 6-sided mirror rotating at 3600 rpm provides a horizontal scan while a rocking single-plane mirror furnishes a vertical scan. A HgCdTe infrared detector, sensitive in the 7- to 14-μm region, receives the object under test's reflected heat and begins the process of converting it into a visual representation of the object's thermal signature. The detector is cooled by a Dewar assembly containing a renewable quantity of liquid nitrogen to ensure a good signal-to-noise ratio.

An enhancement and amplification system processes the detector's signal, which then goes through a temperature-reference control and into the unit's memory. The final thermal image (photos, **(b)**) is constructed in the system's memory as the scan mirrors traverse the test object and is displayed on the built-in CRT monitor. Each horizontal and vertical scan takes 2 sec.

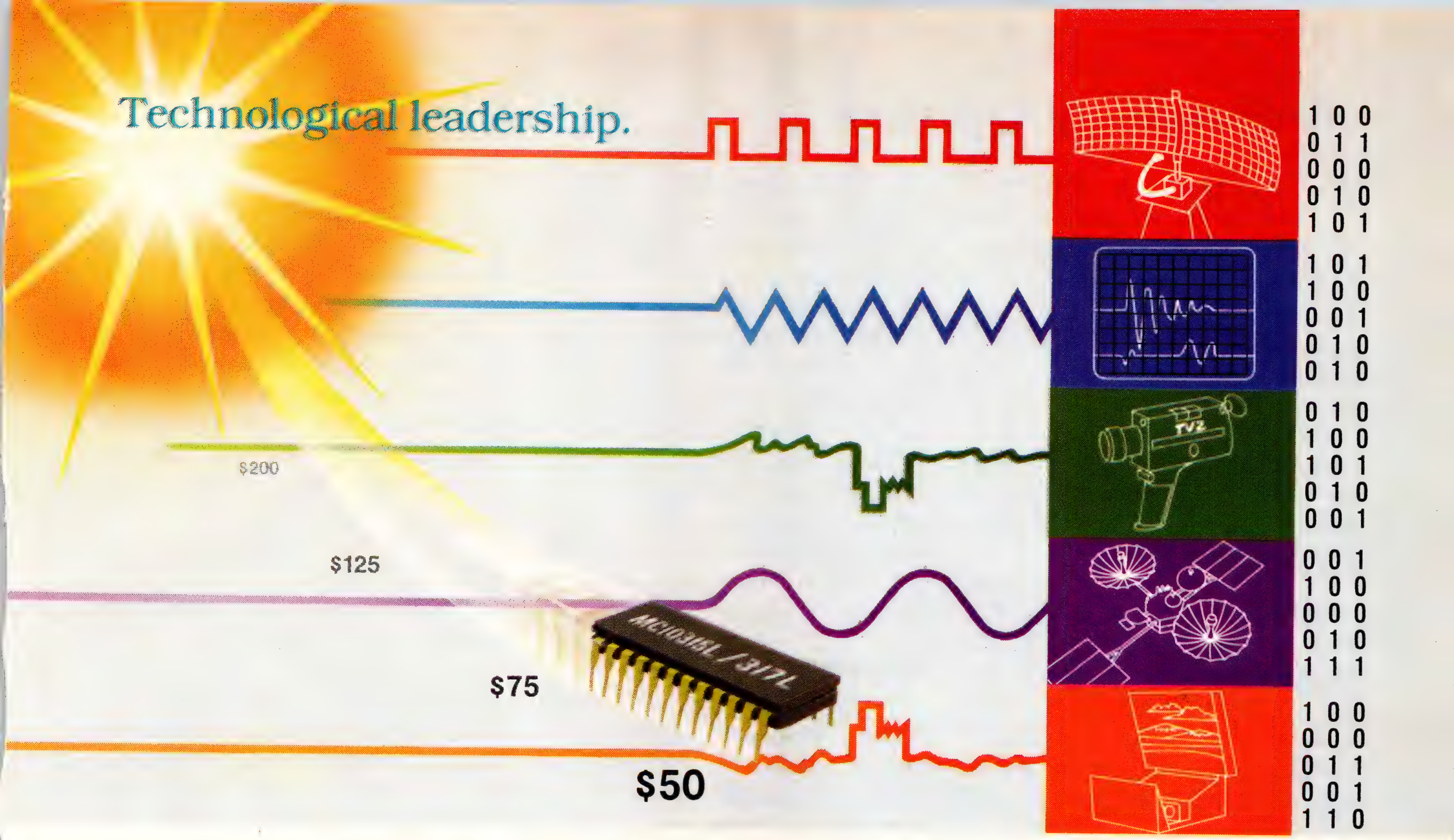
In addition to the device under test's thermal pattern, the displayed image also provides a temperature graph, referenced to a baseline temperature, of the test area crossed by a full-width horizontal cursor. The base-temperature level can be set between −27 and +297°C; system sensitivity can be adjusted to as low as 0.5°C per graduation.

The thermal-imaging system is calibrated using a black-body-radiation source traceable to the National Bureau of Standards; as an additional feature, the stored thermal image can be magnified as much as four times using the digital image-processor/memory system's quartering function. An optional color quantizer converts the black-and-white gray-scale thermal image into a 10-color spectrum.

UTI Instruments's (Sunnyvale, CA) newest system, the Model CCT 9000 computerized color thermograph, utilizes a 13-in. high-resolution RGB color monitor to display temperature gradients measured to 0.1°C. Featuring automatic drift and calibration control, the μP-based unit provides such features as 640×512 RAM storage capable of holding more than 300,000 picture elements, post-processing of image data, image averaging, digital temperature readout, 16× software-based image magnification (with additional 2.5× close-up lens), and optional disk storage and IEEE-488 interface. Furnishing a 16-color temperature gradient, the system provides three viewing modes: the thermal image of the device under test, a RAM-stored reference image or the difference between the two.



Speeding thermal design analysis of complex electronic assemblies, *UTI Instruments's Model 900 thermal-imaging system* ***(a)*** *at Lockheed-California's Thermography Test Lab can furnish an instant photographic image* ***(b)*** *of the device under test's thermal profile, including a temperature graph of points along a cursor line.*



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"How thermography works").

Utilized as an integral part of preproduction analysis of avionics and electronic-systems components, the Lockheed-California system tests engineering models that duplicate actual production units as closely as possible, according to Richard W Sherman, supervisor of ASW-avionics quality engineering, and John P Ketrick, a senior electronics engineer at the Burbank, CA firm.

"It has proven to be a fast, thorough means of analyzing the thermal characteristics of new designs as they are tested in the engineering-model stage," Sherman reports. "Excessive-temperature problems—or even potential trouble spots that might go undiscovered with traditional test techniques—are far less likely to escape into the production cycle. Also, the thermal behavior of nonproblem areas can be easily studied for a greater understanding of a circuit's operational characteristics."

In addition to the electronic systems it develops in-house, Lockheed-California also tests many of the electrical and avionics devices built to its specifications by subcontractors. The Quality Assurance Lab also uses thermal imaging to test in-service systems and components requiring design review after a pattern of failures appears under field conditions.

Performing operational tests

In every case, though, the goal is to test a device under operational or burn-in conditions, Sherman and Ketrick emphasize. Thus, to gain data that's as true as possible to actual operating conditions, the Lab tests assemblies in their operating environment.

A pc-board assembly, for example, is tested in its installed position in the parent electronic unit—not merely under a simulated electrical load. When the board reaches operating temperature, it's removed from the parent unit and placed immediately in a prefocused position in front of the thermal-imaging unit. Four separate scans are then performed at 5-sec intervals and retained in the system's memory.

To compensate for unavoidable cooling that results when power is turned off and the board removed from the parent assembly, the Lab uses a digital timer to measure the elapsed time from power disconnect to the first infrared scan. The temperature variations noted over the 20-sec scan period are then extrapolated back, via an exponen-

Is thermal imaging cost effective?

Considering the relatively high cost of thermal-imaging equipment ($50,000 or more), can designers justify the use of these systems to replace traditional thermocouple-based testing techniques? Direct cost comparisons are difficult to make, but Lockheed-California's Richard Sherman and John Ketrick provide ballpark figures that illustrate the cost trade-offs involved in the two techniques.

Thermal imaging's cost benefits fall under three major categories: test setup and teardown costs, the cost per item of data and the quality of data.

Consider, therefore, a typical conventional test in which 50 thermocouples are applied to a pc-board assembly. Three man-days would probably be required for setup, subsequent teardown and cleanup. Assuming a labor rate of $30 per hr, the test would cost approximately $720. In contrast, a thermographic examination of the same assembly could be completed in approximately 20 min, with hard-copy test-result documentation. The result? A net savings of more than $700 for the thermal-imaging approach.

No meaningful cost comparisons between the two methods in terms of data quantity (and cost per item of data) can be made because one thermal image produces 262k data points in 2 sec. And although you might not need all that data, its sheer magnitude constitutes a substantial cost benefit.

Direct cost comparisons of data quality beteween the two methods are also difficult to make. But because no transducer mass comes into contact with the device under test in thermal imaging, greater data accuracy results. Furthermore, no engineering analysis is required in thermography to factor out the inherent errors involved in the thermocouple approach. And with thermal imaging, you don't have to repeat tests to verify test results.

Thus, although each method's cost per item of data and data quality are difficult to quantify, Sherman and Ketrick still claim an attractive cost benefit for thermography, based solely on test setup and teardown. Using the aforementioned test example, thermal imaging involving three design iterations would therefore produce a savings of more than $2000 compared with thermocouple testing.

The bottom line, according to Sherman and Ketrick, is that thermography provides an investment payback at approximately the 25th design project—assuming equipment cost of $50,000 for a basic system. And the technique's other, less tangible advantages, such as its greater amount of data, advance the break-even point even further.

One final cost benefit is that the equipment doesn't require special training or skills to operate: Competent electronic technicians are usually able to begin thermal testing after merely familiarizing themselves with equipment controls and their effect on the thermal image.

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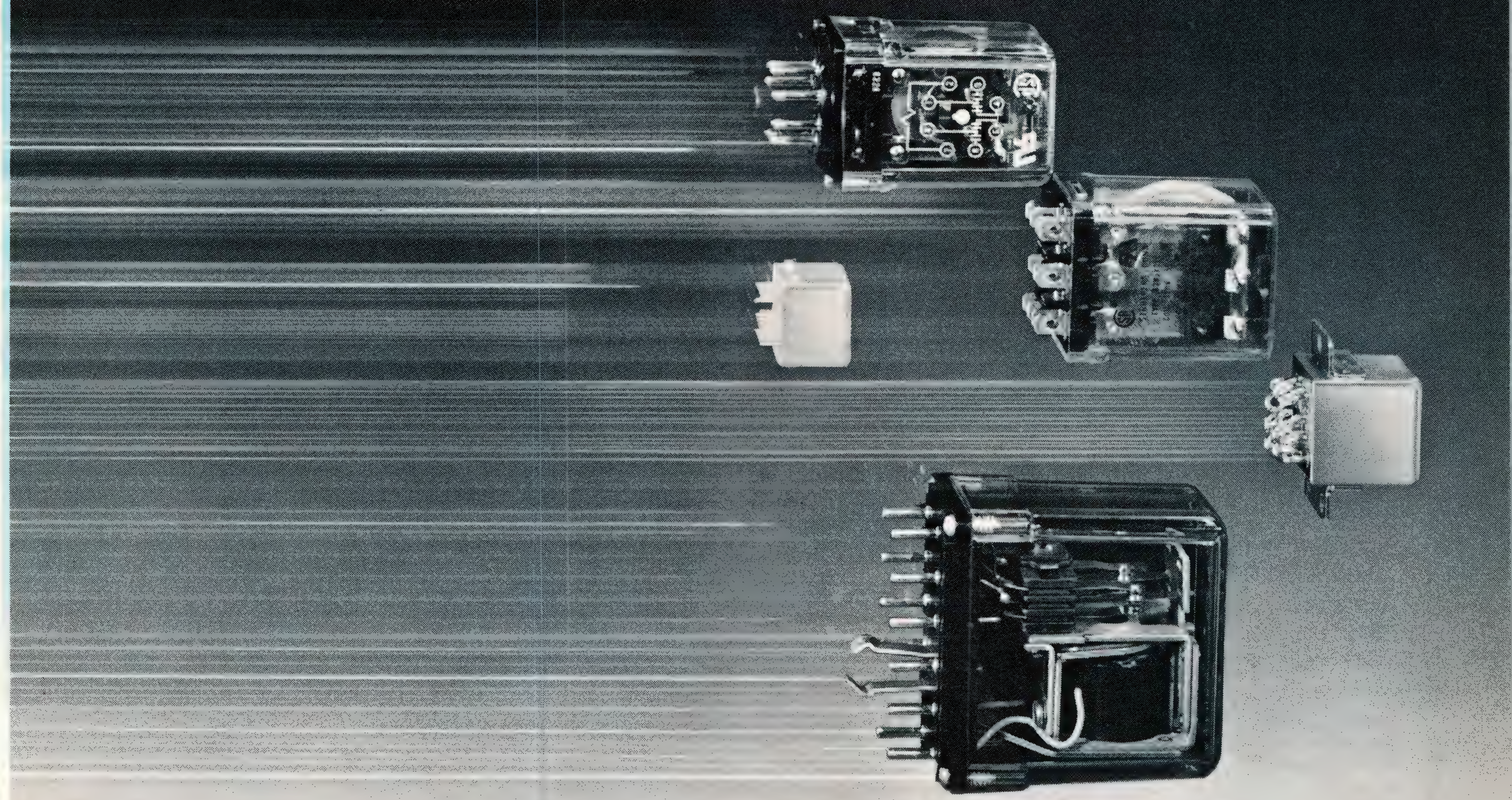

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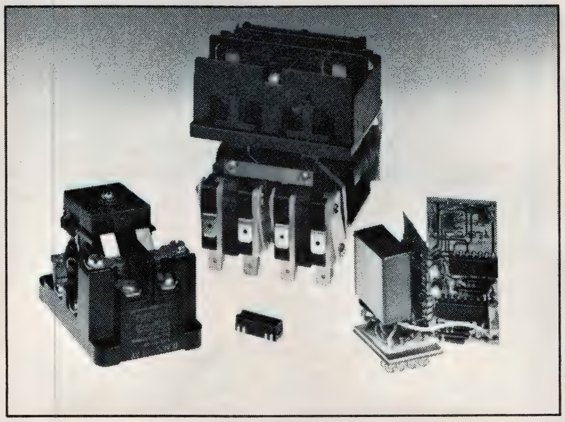

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Technology

tial curve-fitting program, to obtain a temperature-decay rate expressed in degrees Celsius per second.

"With this method," Sherman says, "designers are able to arrive at a profile of the board's thermal condition in its actual operating surroundings. When necessary, standard thermocouples are used in a few sample areas to verify the accuracy of the cool-down-compensation calculations as well as component surface temperatures."

Sherman and Ketrick report, however, less than 0.5°C average variation between data from the two temperature-measuring methods. "Because of this high degree of predictability," Sherman says, "quality-assurance engineers have become more confident in the results of thermal imaging and rarely feel the need for substantiation of the results."

Partly in response to Lockheed-California's testing program, its customers are also placing increased emphasis on thermographic testing, and several have specifically requested thermal-imaging analysis of in-service problems.

Expanding applications

Although the Lockheed-California experience has involved commercial and military aircraft systems, Sherman and Ketrick emphasize thermal imaging's usefulness in many other areas of electronic design involving complex printed-wiring assemblies. The technique has also been utilized in nonelectronic applications—to examine thermal-adhesive bonds, composite honeycomb structures and glass-laminate aircraft windshields, for example.

"Thermal imaging as a design technique is still a long way from its full potential in high-technology industries," Sherman concludes. "But as its use spreads, so no doubt will its applications." **EDN**

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HA-5064B	3 mV	200 pA	0.8 mA	Quad	
HA-5082B	2 mV	200 pA	5.6 mA	Dual	Industry Standard JFET Input Op Amps
HA-5084B	2 mV	200 pA	11 mA	Quad	
HA-5130	25 μV	2 nA	1.3 mA	Single	Higher Precision Higher Speed Op-07 Direct Replacement
HA-5135	75 μV	4 nA	1.7 mA	Single	
HA-5141A	2 mV	75 nA	65 μA	Single	Highest Speed Micropower Op Amps Available
HA-5142A	2 mV	75 nA	130 μA	Dual	
HA-5144A	3 mV	75 nA	260 μA	Quad	
HA-5170	0.5 mV	60 pA	2.1 mA	Single	Low Drift Low Noise JFET Op Amp
HA-5180	3 mV	1 pA	1 mA	Single	Ultra Low Bias Current JFET Input Op Amps
HA-5180A	0.5 mV	1 pA	1 mA	Single	
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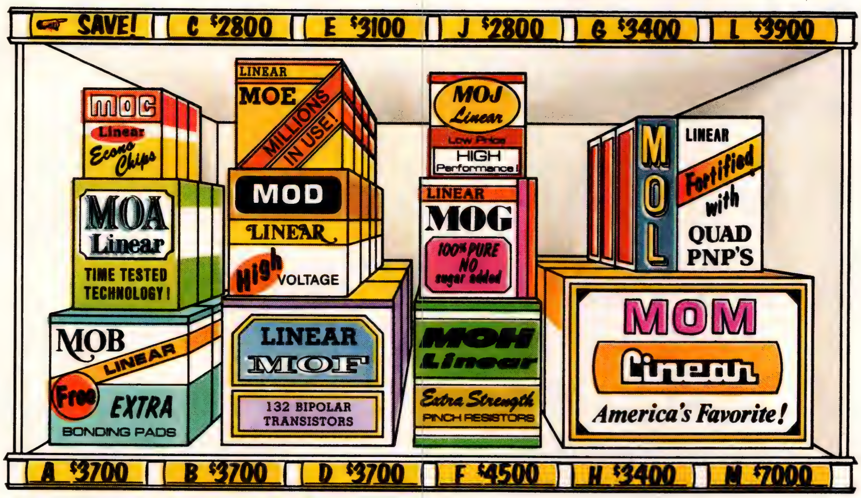

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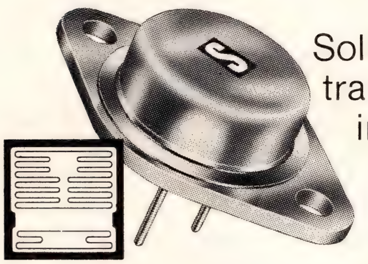

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Technology Update

AM-stereo technology gains momentum, but no industry standard is in sight

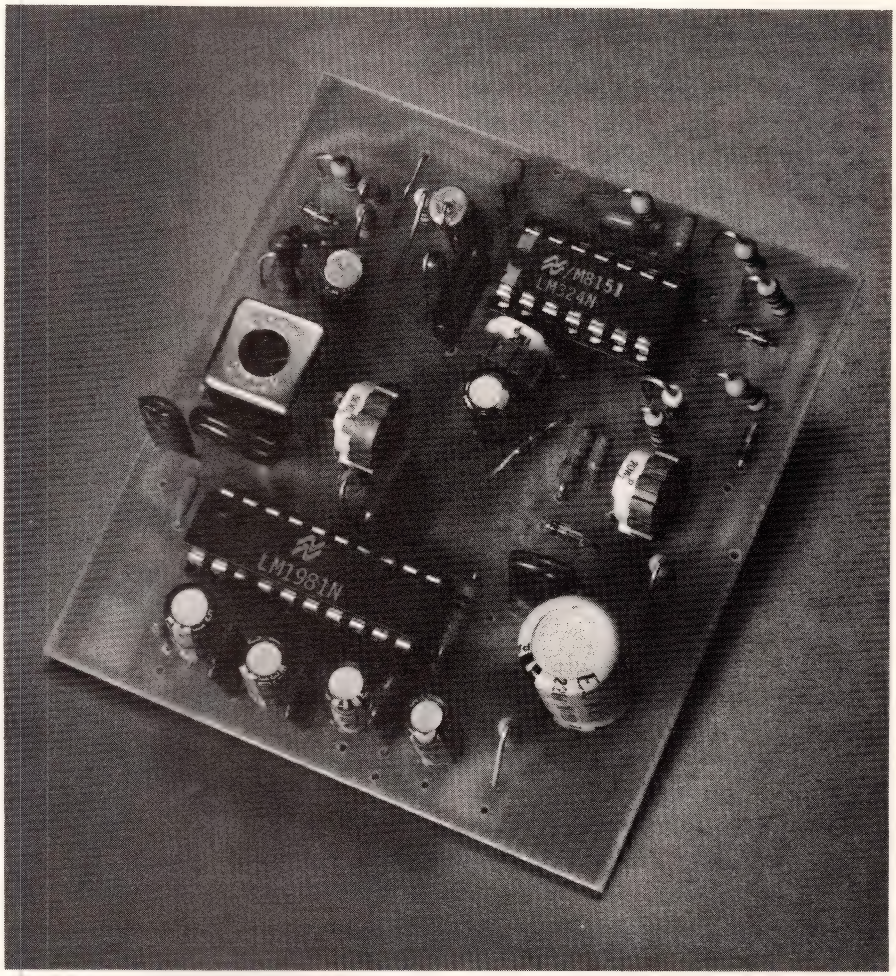
John Tsantes, Eastern Editor

Despite the increased emphasis radio broadcasters, transmission-equipment suppliers, receiver manufacturers and the semiconductor industry are placing on AM stereo, the adoption of a universally accepted standard is no closer to realization today than it was 6 months ago, when the Federal Communications Commission (FCC) elected not to select a standard from among the five competing systems.

Indeed, the FCC's controversial "marketplace decision" might not in any event lead to market standardization on the best system; possibly, no system will achieve that status. And because the decision has given rise to a significant increase in competitive promotion among the five proponents, it's even possible that the company with the largest advertising budget and best promotional campaign will see its standard adopted, regardless of its system's technical performance.

The only positive aspect emerging from this FCC-created mess is that all five systems—from Belar/RCA, Harris, Kahn/Hazeltine, Magnavox and Motorola—are technically capable of producing AM stereo. Several IC manufacturers, recognizing this fact, are producing devices that accommodate one or more of the systems. Therefore, if you're involved in circuit or equipment design specifically intended for AM-stereo applications, rest assured that the basic technology is solid. But also realize that your efforts might be in vain if the system you're backing doesn't become a de facto standard.

The AM-stereo saga began on June 22, 1977, when the FCC adopted a Notice of Inquiry in response to petitions for rulemaking concerning AM stereophonic broadcasting. As explained in that Notice, the agency considers several system objectives important in the development of AM-stereo broadcast service.



Convert a monophonic radio to AM stereo *by combining National Semiconductor's LM1981 IC with several peripheral chips.*

These objectives include compatibility with existing AM broadcast (monophonic) receivers, transmitters and antennas; compliance with existing AM bandwidth limitations to miminize interference; simplicity of design and reasonable cost for receiving equipment; no reduction in service area or loudness for either monophonic or stereo reception; satisfactory stereo service for nighttime skywave reception; and simple administrative procedures for implementing AM stereo upon approval. Except for the last objective, all AM-stereo proponents have met these requirements to a satisfactory degree, in the FCC's view.

However, the key word is *satisfactory*. Some of the original design objectives are interdependent. Occupied bandwidth, for instance, depends on the stereo signal's frequency-response range. In addition, the need for uniform loudness of the AM signal when received on a conventional monophonic receiver might not permit full stereo separation under certain program conditions. And the monophonic-compatibility requirement compromises stereo separation sim-

Awaiting Delco's blessing

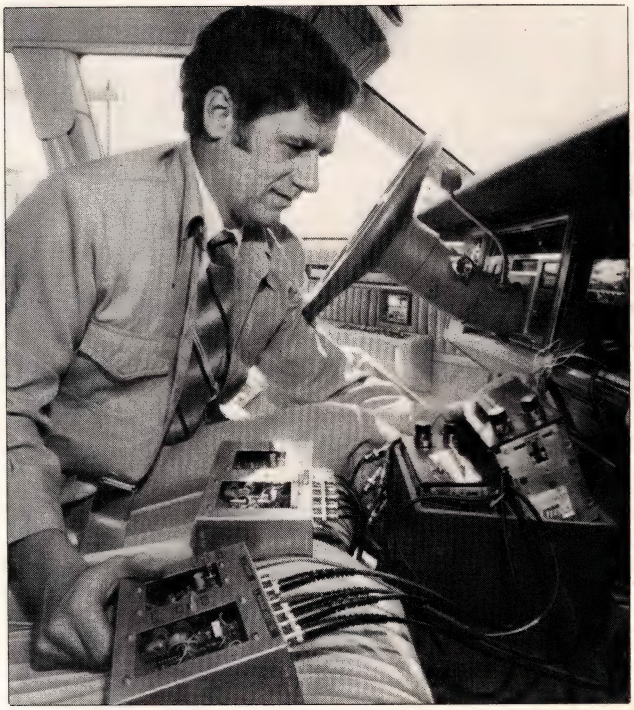
A potential spur to a decisive market decision on AM stereo might come from General Motors's Delco Div, which has begun to evaluate the various systems for possible automotive-receiver use. However, Delco's projected July 1982 decision date has come and gone, and no decision has yet been made. Still, when a decision comes, many observers feel that it will set up a de facto standard.

Unfortunately, Delco's eventual decision might not indeed be decisive. Why? For one, Delco is currently evaluating only the Harris, Magnavox and Motorola systems. According to director of engineering R J McMillin, Belar has apparently dropped out of contention, and Kahn has not answered Delco's inquiries. Thus, the truly best system might not even be under evaluation. In addition, each AM-stereo proponent maintains that it will continue pushing its own system, even if it's not chosen by Delco.

As of this writing (August), Delco sees no system having a strong advantage compared with the others. Furthermore, although some systems appear more complicated than others, McMillin sees no strong reason to discriminate on the basis of that criterion. And he adds that despite claims of higher system costs for some designs, cost will play only a small role in his firm's decision.

Instead, mobile-reception capability will be the key. Delco will obviously choose the system that can perform best in a moving automobile. Assuming that the firm chooses one system within the next few months, and assuming that the rest of the industry goes along with this decision, AM-stereo radios will not appear in cars before model year 1984.

McMillin has stated no personal preference for any of the AM-stereo systems. But he admits that he would have liked it better had the FCC made the decision for him.

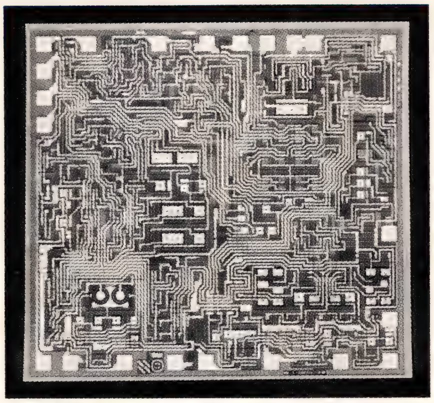


Three systems *are being evaluated by General Motors's Delco Div for automobile applications. Delco considers performance in a moving vehicle the most important evaluation parameter.*

ply because it's more difficult to simultaneously satisfy two design requirements than one.

All use same decoding scheme

Despite the various approaches the five proponents have taken to satisfy the FCC's requirements, all rely on the same basic encoding technique. In it, two separate program-information signals get transmitted from the studio to the receiver, one containing the Left (L) information and the other the Right (R). To achieve compatible reception of both channels on a monophonic receiver, the two signals get added together (L+R) for transmission. A second channel, frequently termed the stereo subchannel, carries the difference (L−R) information.



An AM-stereo decoder, *National Semiconductor's LM1981 accommodates the Magnavox system and sells for $1.25 (50,000).*

The L+R signal gets amplitude-modulated by the usual technique, thereby achieving mono-AM compatibility. The L−R information is either phase- or frequency-modulated (depending on the scheme under consideration) and used by the stereo receiver to separate the L+R signal back into the original left- and right-channel programming.

For instance, in the Belar system, the sum signal is applied to the modulation circuitry of a conventional AM transmitter, while the difference signal angularly modulates the RF carrier. The angular modulation exhibits FM characteristics for low audio frequencies and phase-modulation (PM) characteristics for mid-audio frequencies. This FM-to-PM changeover is accomplished through a pre-emphasis network, which boosts the modulating signal. The carrier's maximum frequency deviation varies from 312.5 Hz at low frequencies to 6250 Hz at higher ones. The Belar

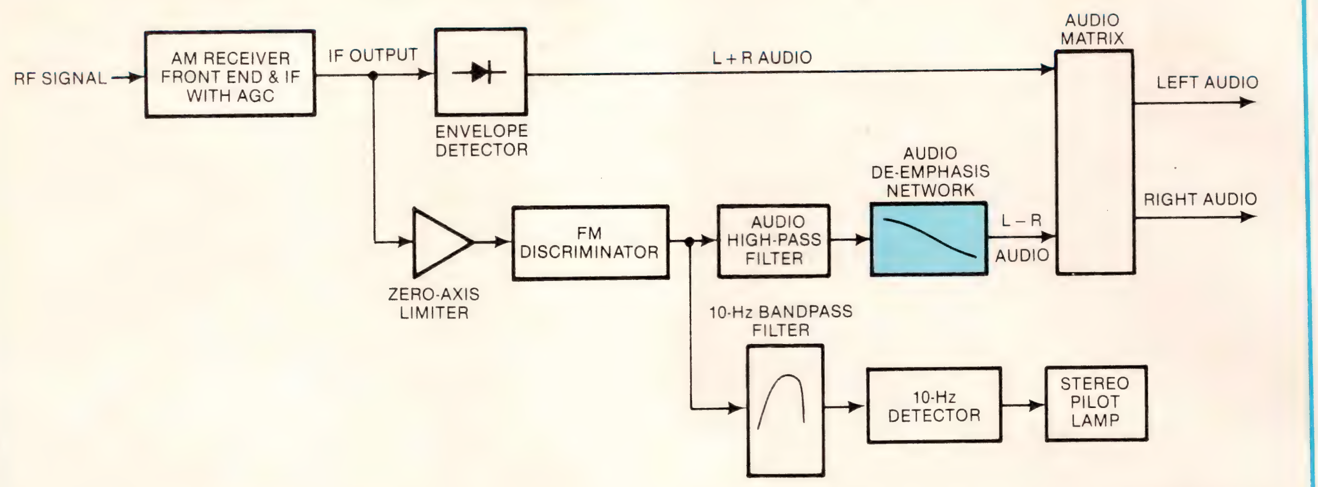


Fig 1—A de-emphasis network *in the Belar AM-stereo system attenuates the modulating signal and also reduces detected noise.*

system also requires a 10-Hz pilot tone, which the receiver can use to indicate reception of AM stereo.

Belar's proposed decoding system is essentially complementary to the encoding method used in the transmitter (**Fig 1**). In it, a conventional diode detector detects the L+R signal in the envelope, and a limited IF signal (free of amplitude modulation) gets applied to an FM discriminator. An audio high-pass filter rejects the pilot tone. The receiver's de-emphasis network is the complement of the transmitter's pre-emphasis network; in it, the L+R and L−R signals are applied to an audio matrix that produces the original left- and right-channel audio signals. The discriminator's output goes to a bandpass filter centered on 10 Hz, so most program material and noise are removed from around the pilot tone. The presence of a signal at the output of this filter then triggers a stereo-indication mechanism.

(Ed Note: Only decoder circuits for the various systems are illustrated. We feel that more EDN readers are involved in receiver designs than in transmitters.)

The only linear system

The Harris system, in contrast to the Belar scheme, modulates two carriers, an in-phase (I) and quadrature (Q) carrier, which are

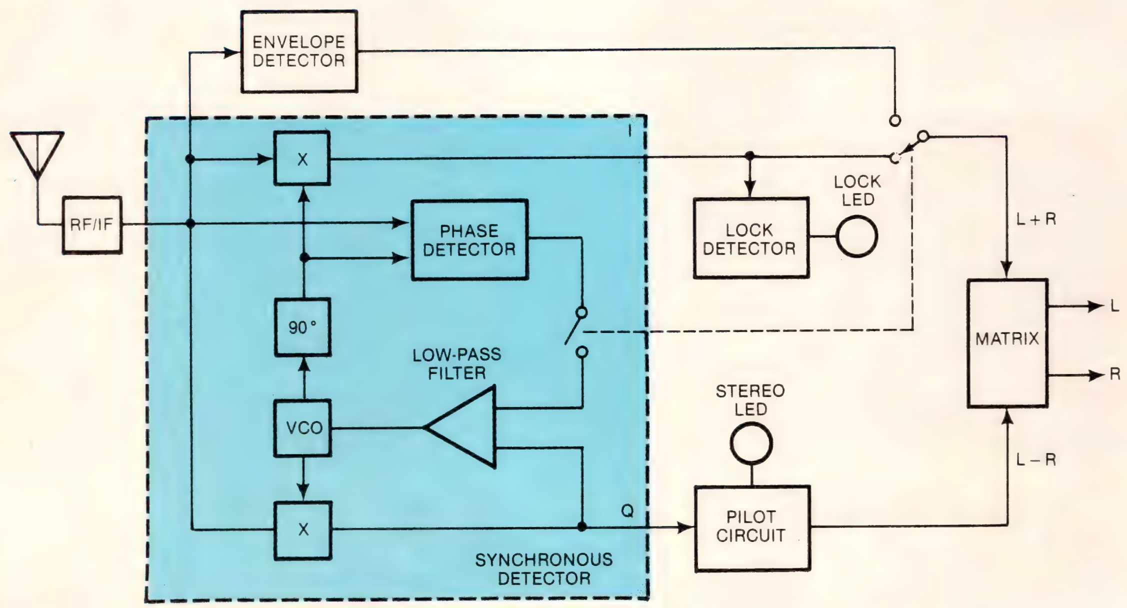


Fig 2—The only linear AM-stereo decoder, *from Harris, might be technically superior to the other proposed systems. But the Harris transmission system does produce higher harmonic distortion in conventional envelope-detector monophonic receivers.*

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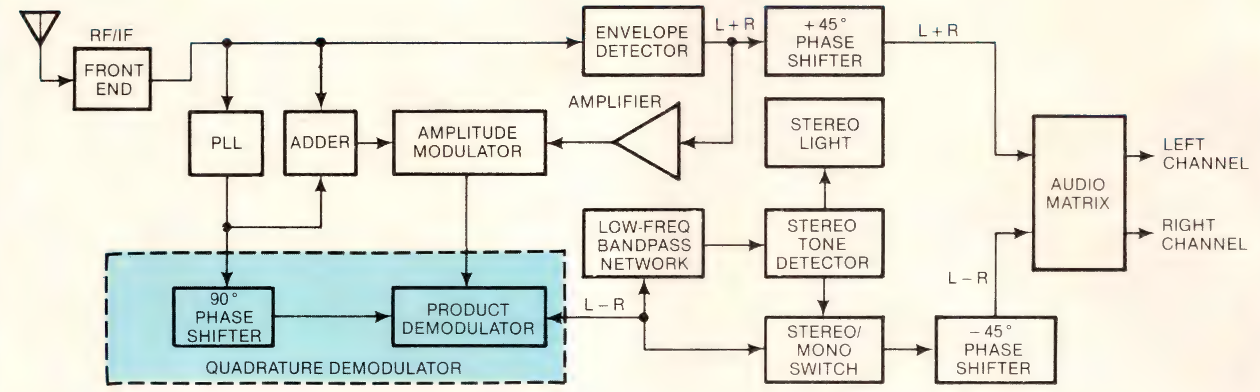

Fig 3—Phase modulation carries the stereo information *in the Kahn/Hazeltine system. This decoder receives the stereo, but two monophonic radios tuned slightly off-frequency also produce the same stereo effect.*

90° out of phase. The in-phase carrier gets modulated by the L+R signal, while the L−R signal modulates the quadrature carrier. The modulated signals then combine into one signal whose phase and amplitude modulate the transmitted signal's phase and amplitude.

You can consider the Harris system as two carriers separated by an angle that can vary from 90 to 30°. The left-channel signal modulates one of these carriers; the right channel, the other. The variable angle between the carriers is directly related to the L−R gain-reduction factor. (Gain reduction is needed to provide monophonic compatibility and does not affect linearity.)

To properly decode the Harris signal at the receiver, the instantaneous gain used in the L−R channel must be transmitted with the signal. This requirement is accomplished via a varying pilot-tone frequency that changes from 55 to 96 Hz, depending on the L−R signal's gain reduction.

Harris calls its system V-CPM, standing for variable compatible-phase multiplex. To receive a V-CPM transmission in stereo, a quadrature AM (QAM) receiver recovers the signal's I and Q audio-frequency components **(Fig 2)**. A phase-locked-loop PM detector recovers the pilot signal and the frequency-modulated gain information. The recovered pilot gets subtracted from the Q signal to eliminate it from the audio output, and the Q channel's gain is then increased by the same factor it was reduced by in the transmitter. The I and Q signals can then go to an audio matrix that recovers the left- and right-channel audio signals.

Two radios produce stereo effect

The Kahn/Hazeltine system, meanwhile, uses phase modulation to carry the stereo information on the sidebands. Because most of the left-channel stereo information is placed in the lower sideband while the right-channel program is in the upper sideband, this system is termed an independent-sideband (ISB) arrangement.

The system achieves AM-stereo operation by phase-modulating the RF carrier with the L−R signal and then performing amplitude modulation on the result. A 15-Hz pilot tone angle-modulates the carrier by approximately 0.1 radian.

Although the Kahn/Hazeltine signal can be decoded by one receiver **(Fig 3)**, the stereo effect can also emerge through two radios, one tuned slightly above the center frequency and one slightly below. Several radio stations across the country have already installed Kahn AM-stereo exciters for field testing, and listeners are decoding the stereo signal in just this manner.

Envelope modulation

The Magnavox system is an AM/PM configuration that uses envelope modulation for the L+R information and linear phase modulation for the L−R information. Phase-deviation equals 1 radian peak, and a 5-Hz subaudible tone gets frequency-modulated onto the carrier with a deviation of approximately 20 Hz to provide stereo identification.)

Magnavox's receiver is a single-IF system using a standard envelope detector for the AM channel. Its automatic gain control can hold L+R output nearly constant over a wide range of RF signal levels, allowing proper dematrixing of the L+R and L−R signals. The simplest receiver design for this system **(Fig 4a)** is a nonsynchronous circuit; the PM information can also be recovered by sampling the IF signal, limiting it and detecting it with a phase-locked loop **(Fig 4b)**.

The stereo-identification tone in the Magnavox configuration is regenerated by recovering the audio tone present between the main voltage-controlled oscillator and the loop filter (present as a byproduct of the phase-detection

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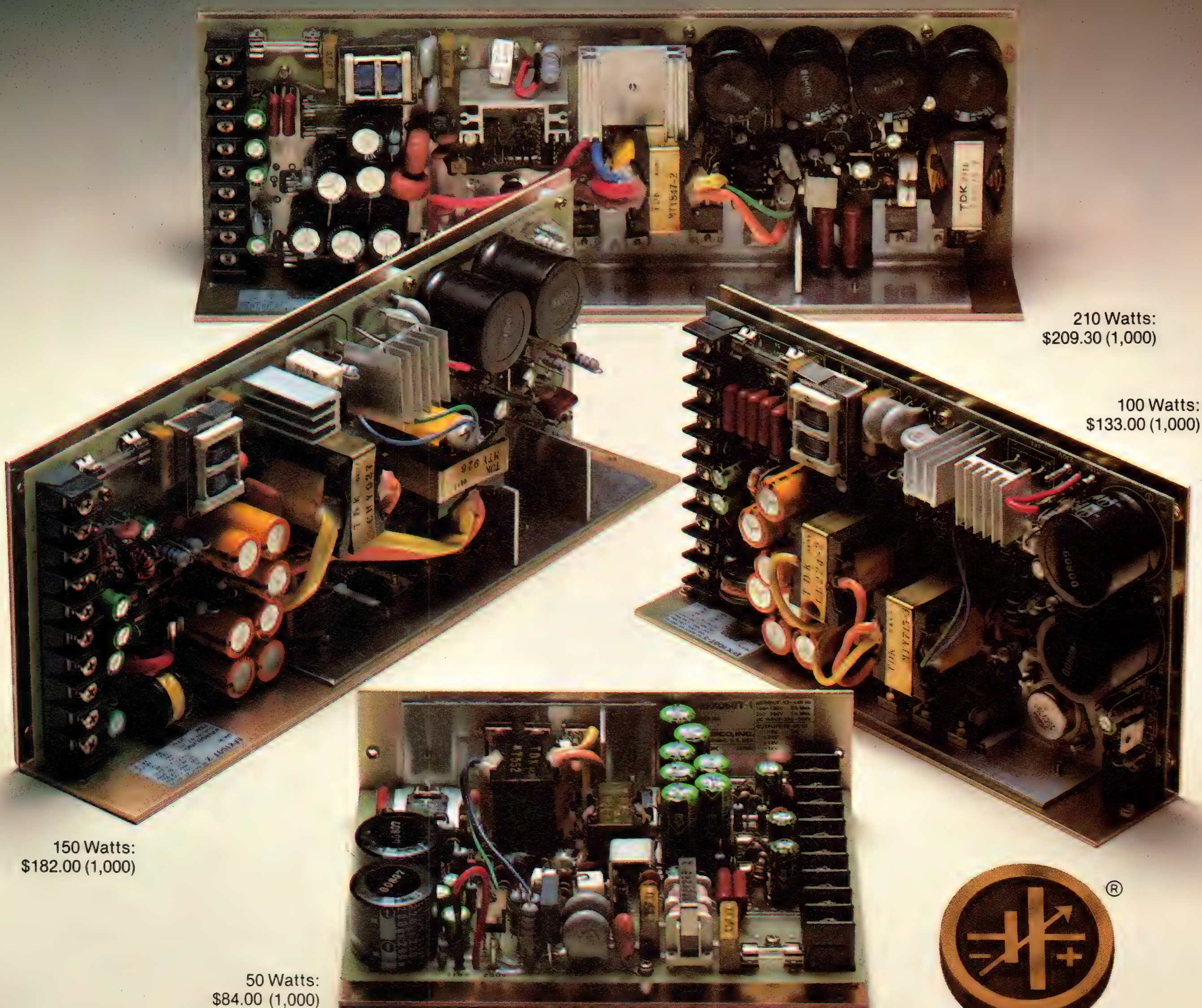

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process), and passing it through a tone detector to drive an indicator. An automatic mode switch provides switching between mono and stereo and is driven by the stereo-ID circuitry.

Linearity lost for compatibility

The final system, Motorola's C-QUAM (compatible quadrature AM), uses two amplitude-modulated RF carriers that are 90° out of phase: The L+R signal modulates one; the L−R signal, the other. Unmodified, such a system is linear, but the amplitude of the resultant signal is not fully compatible with monophonic envelope-detector receivers. Therefore, to achieve a better degree of compatibility, the combined signal is first hard-limited and then remodulated with the L+R signal. However, although this scheme produces monophonic compatibility, it destroys the system's linearity.

According to Motorola, any suitable stereophonic audio processor and matrix can generate the necessary sum and difference information. The received compatible quadrature signal is merely one that has been modulated by the cosine of its relative phase-angle information and is also a compatible envelope-detector signal. Therefore, the Motorola system can decode sum information with either an envelope detector or a synchronous detector that's inversely modulated by the cosine of the phase modulation. Similarly, it can decode difference information with a synchronous quadrature demodulator that's inversely modulated by the cosine of the phase modulations.

According to Motorola, many decoding methods exist because

$$L-R=S\tan\theta=S\sin\theta/\cos\theta$$

when S is the AM monaural signal and equal to L+R. Hence, any sequence of operations that results in L−R is a valid decoding algorithm. Even non-PLL decoders are allowed, because a discriminator/integrator/tangent-function sequence results in the L−R signal.

Motorola's preferred decoder design **(Fig 5)** uses the synchronous-detector scheme. In the absence of the feedback loop, the in-phase detector would produce $(1+S)\cos\theta$. But the loop makes the in-phase-detector output identical to the envelope-detector output, which also forces the variable gain control to be an inverse-$\cos\theta$ modulator. Therefore, the quadrature phase detector's output becomes the

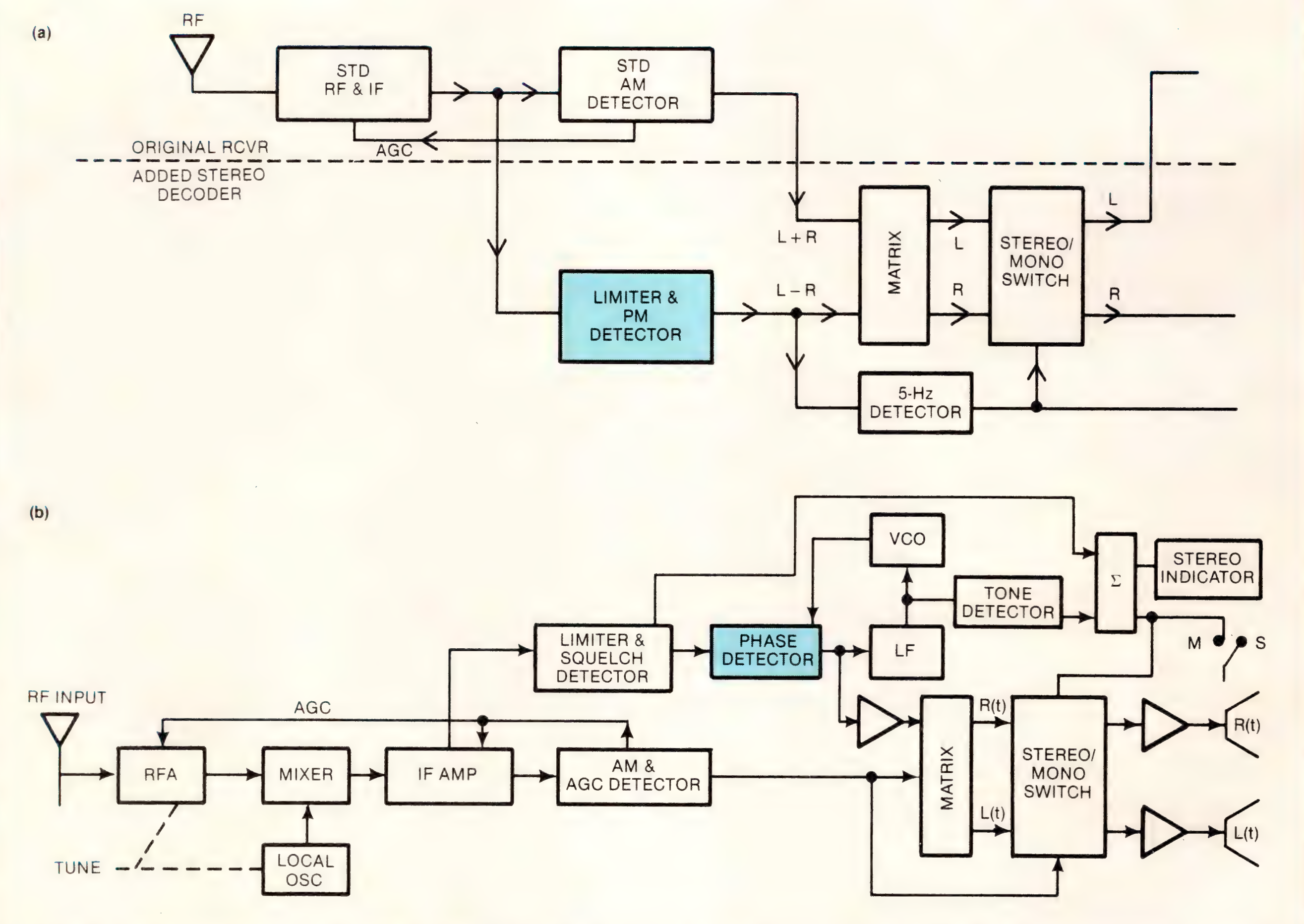
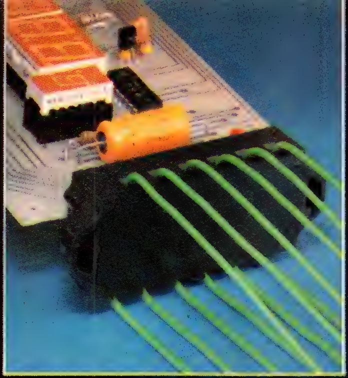


Fig 4—A nonsynchronous circuit (a) *yields a simple decoder for the Magnavox signal. But the PM information can also be recovered by sampling and limiting the IF and detecting it with a phase-locked loop* ***(b).***



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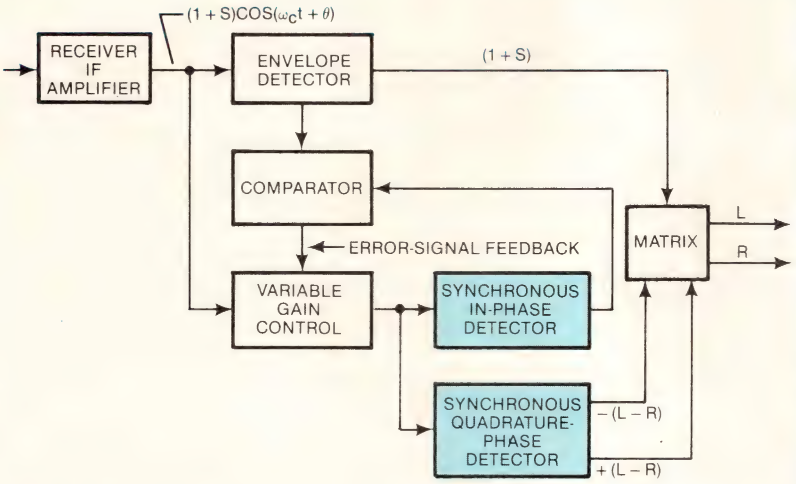
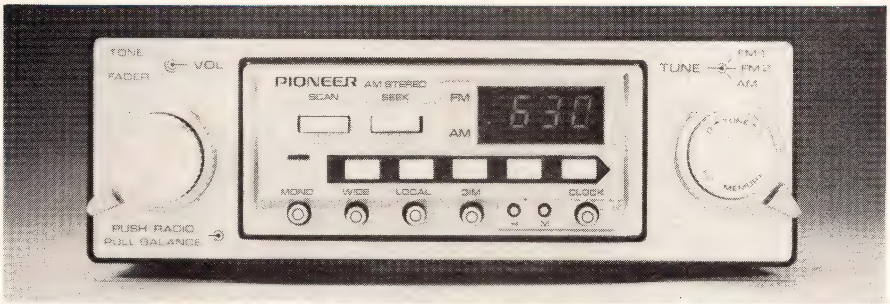


Fig 5—A synchronous detector scheme *is preferred by Motorola to recover its C-QUAM system's signal. The L−R signal should function as the error for the loopback.*



This prototype *of a Magnavox-system AM-stereo receiver, built by Pioneer, uses the National Semiconductor LM1981 decoder IC. (Photo by permission of Pioneer Electronics)*

FCC AM-STEREO EVALUATION TABLE

EVALUATION CATEGORY Numbers in parentheses ( ) indicate the maximum possible scores in the various categories or subcategories.	MAGNAVOX	MOTOROLA	HARRIS	BELAR	KAHN
I MONOPHONIC COMPATIBILITY					
(1) Average Harmonic Distortion (15)	15	9	6	9	12
(2) Mistuning Effects (5)	5	5	5	5	5
II INTERFERENCE CHARACTERISTICS					
(1) Occupied bandwidth (10)	3	4	10	5	6
(2) Protection ratios (10)	7	7	8	1	9
III COVERAGE (Relative to Mono)					
(1) Stereo to mono receiver (5)	5	5	5	5	5
(2) Stereo to stereo receiver (5)	—	—	—	—	—
IV TRANSMITTER STEREO PERFORMANCE					
(1) Distortion (10)	8	8	6	8	4
(2) Frequency response (10)	8	5	5	6	8
(3) Separation (10)	10	10	10	8	3
(4) Noise (10)	6	10	8	6	8
V RECEIVER STEREO PERFORMANCE					
Degradation in stereo performance over that measured at the transmitter, including consideration of directional antenna and propagation degradation (10)	9	8	9	5	5
TOTAL SCORES	76	71	72	58	65

This controversial AM-stereo evaluation table *makes it appear that Magnavox was the FCC's clearcut choice. In fact, the agency now admits that the only thing the table shows is that all systems are capable of producing satisfactory AM stereo.*

desired L−R information. (For maximum performance of PLL decoders, Motorola recommends that L−R be utilized as the error signal for loop lock.)

Choosing the best system

From the foregoing discussion, you can see that choosing the "best" system for AM stereo is no easy task. The responsibility for making this choice has rested with the FCC. But with its March 4, 1982 Report and Order, which decrees that the marketplace is the best arena for evolving a national standard for AM-stereo broadcasting, the FCC considers the entire matter closed.

Many industry observers feel that this decision is total insanity. But the decision has managed to raise each proponent's hopes that its system will gain widespread market approval. As a result, each firm has launched a massive campaign to sway industry opinion.

Typically, such a campaign's paperwork includes a list of technical advantages claimed for the proponent's system and a larger list of claimed disadvantages for competing systems. Also included is a list of comments from various broadcast- and receiver-equipment manufacturers, providing support for the system.

The results to date? No clearcut leader has emerged; all proponents, however, predict eventual victory.

FCC changes its mind

Oddly enough, the FCC at one time had decided on the Magnavox system. But it changed its mind once the other proponents and their supporters voiced opposition.

In its decision for Magnavox, the agency relied heavily on an AM-stereo-system evaluation table prepared by its staff (**table**). However, after receiving industry comments regarding the table's validity, the staff found that some of the original judgment criteria could not be adequately quantified. In some other areas, sufficient data was not available to score the entries in a

meaningful way.

Physicist Dr Joe McNulty of the FCC's Laurel, MD laboratory admits that statistically, you can't tell from the table the difference between two systems 20 points apart in overall rating. "The tests used," he says, "were not independent. You cannot possibly tell from the table which one of the systems is superior." McNulty does assert, however, that the table reveals that all five systems are capable of being implemented.

It was after its second analysis that the FCC decided to back away from its initial findings and not adopt any system. Keep this fact in mind when you're confronted by competitive literature that bases conclusions on the original system-evaluation table.

FCC: Linear system superior

In addition, realize that although the FCC's table has been widely publicized, one fact is less well known: Based on purely technical considerations, the FCC believes that a linear system is far superior to a nonlinear one for the production of AM stereo.

To understand this conclusion, consider that whenever an RF carrier wave gets modulated, sidebands are generated. If the modulating function consists of only linear terms, only simple sum (L+R) and difference (L−R) frequencies appear in those sidebands; no intermodulation products and no sideband components of harmonic order higher than the first can be produced. In addition, no out-of-band emissions occur, and the total bandwidth required is only twice the highest modulating frequency.

If the modulating function is nonlinear, though, intermodulation products and higher order sidebands result, and these emissions must be preserved to prevent excessive signal distortion. Therefore, to achieve the same frequency response without distortion, the bandwidth required for a nonlinear system must be at least twice that of a linear one.

In the case of AM stereo, bandwidth limitations arise because of the FCC's frequency allocations. As a result, in a nonlinear system, the maximum audio frequency at which stereo separation can be attained is at best only half that of a linear AM-stereo system. Therefore, significant advantages of an ideal linear AM-stereo broadcasting system include no out-of-band emissions, no intermodulation products, a full audio range (50 to 15,000 Hz), greatest compatibility with the use of synchronous detectors, full compatibility with monophonic receivers using these detectors, and the ability of receivers to use the same type of detector in both the L+R and L−R channels.

The linear drawback

Based on the FCC's research, then, the linear Harris system is technically superior to the rest, strictly in terms of AM-stereo production. Its one drawback is its lack of compatibility with conventional monophonic AM envelope detectors. That is, if you try to receive a Harris-system full-stereo signal on a conventional mono-AM unit, the resulting harmonic distortion equals 4.3%. Therefore, the Harris system is only approximately 96% compatible with mono AM.

Although opponents have cited this fact as a strong mark against the Harris system, others argue that a linear system's advantages far outweigh the fault, particularly because mono AM is badly distorted anyway. In addition, although the FCC's McNulty admits that the Harris system might prove more costly to produce because it requires a companding pilot tone, its ability to use the same detector in the L+R and L−R channels helps compensate.

McNulty and his colleagues, then, had hoped that the FCC commissioners would choose a linear system. But he admits that the final judgment was based on nontechnical as well as technical grounds.

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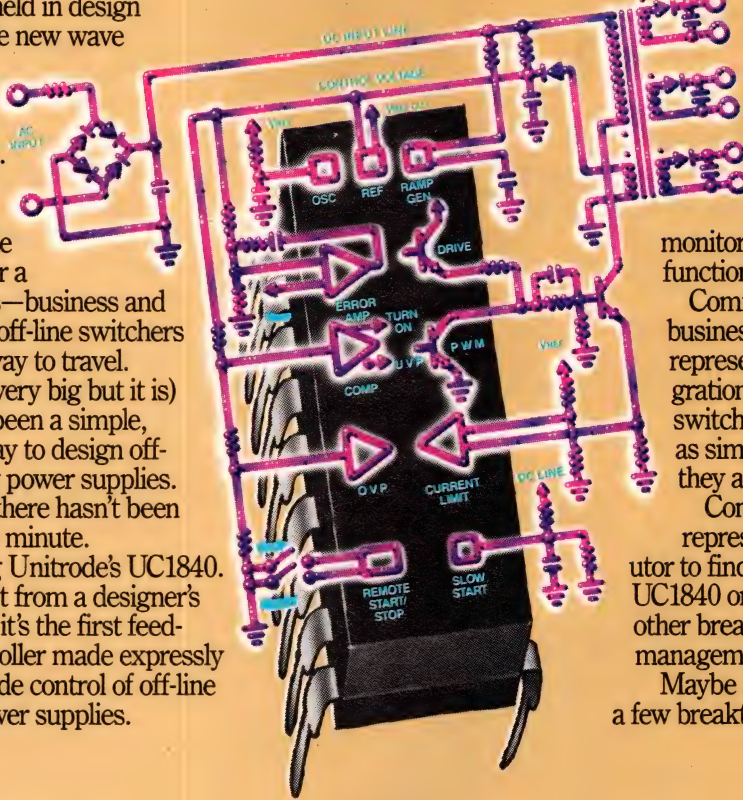

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"The Commission must look at economic, legal, technical and other criteria before making a decision," McNulty says. "I wasn't surprised at its decision because I was aware of the factors that went into it."

IC makers ready stereo chips

Fortunately, the FCC's indecision has not spread to the semiconductor industry. There, a few companies have already announced ICs designed to decode several of the proposed systems' signals.

For instance, Motorola has developed the 20-pin MC13020P to decode its own C-QUAM system. The circuit, implemented in a standard bipolar linear process, provides both AM-stereo decoding and pilot-tone detection.

Under design for slightly more than 1 yr, the device requires no adjustments or coils and only a few peripheral components to achieve decoding. It employs full-wave envelope-signal detection at all times for the L+R signal and only decodes L−R signals in the presence of valid stereo transmission. A 25-Hz pilot presence is required to receive the L−R signal, and pilot-acquisition time equals 300 msec for strong signals.

The MC13020P output's total harmonic distortion (THD) has been preliminarily specified as 0.5% for mono and 1.0% for stereo. Channel separation equals 30 dB, and the device operates from a 6 to 12V dc supply. An internal level detector can be used as an automatic-gain-control source. Motorola expects to sell the device for about $1.50 in very large quantities.

National Semiconductor, meanwhile, having gotten into the act in the early stages of the AM-stereo talks, is backing the Magnavox system with its LM1981 stereo-decoder chip. According to Dan Shockey, product marketing engineer, the firm's analysis was based on cost and system complexity. He believes that the Magnavox pilot tone is easier to detect because it's

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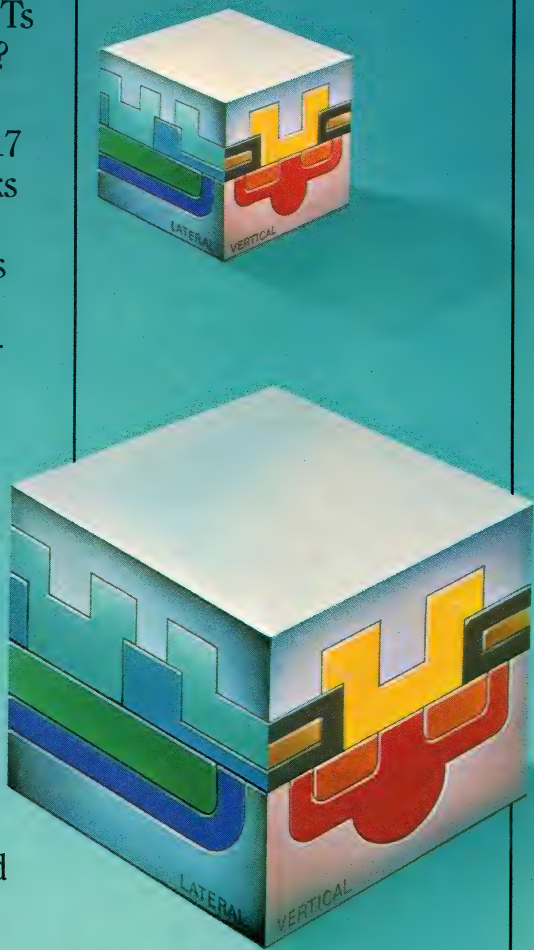

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about 12 dB higher than the audio, making stereo decoding and identification much easier.

The 20-pin LM1981 is being produced on National's new 5-in.-wafer bipolar line. The device is designed to decode stereo information that's amplitude- and angle-modulated on an AM-stereo broadcast carrier. As a result, Shockey claims it can also be used in other systems with very little modification of system components.

The part can accept a 455-kHz (or 262-kHz) IF-amplifier output and can amplitude-detect the L+R mono signal. It also limits, detects and conditions the L−R signal and combines both in a matrix to produce the left- and right-channel audio output.

Other features include an excess-phase detector, stereo-pilot-tone output, stereo/mono-blend function, output S/H circuits and an internally regulated reference voltage. Stereo separation specs at 30 dB; THD, at 0.2% in mono and 0.4% in stereo. Operating voltage can range over 8 to 18V dc.

The LM1981 is available now and sells for $1.25 (50,000). According to Shockey, the total cost of adding AM-stereo capability to equipment that already includes FM stereo should run about $3 or $4.

Although National is focusing on getting the Magnavox-system chip ready for production, it's also anxious to get started on a second-generation part. Shockey says that this design will include more functions, pilot-tone decoding and additional noise protection.

Meanwhile, although few details are available on Sanyo's Magnavox-compatible LA1900 IC, Toshiba's TA7406P is slated for use on the company's own receivers and will also be offered for outside sales.

The bipolar TA7406P incorporates a limiting amplifier, PM detector, pilot-tone-signal detector and automatic mono/stereo switching in an unusual 16-pin zigzag in-line package (ZIP) style. The device, which operates from a 4 to 15V dc supply, specs 0.5% THD, stereo separation of more than 35 dB and a built-in voltage-controlled amplifier for level equalization. According to Toshiba, it can be applied to the Belar system by adding a few extra components.

Meanwhile, Harris Semiconductor, to no one's surprise, is backing its own AM-stereo system with the HS-3604 IC. This 24-pin-ceramic-DIP AM-stereo demodulator uses pure synchronous detection to take full advantage of the Harris system's linear characteristics.

The device accepts an IF signal (100 kHz to 1 MHz) and produces left- and right-channel outputs. Additional outputs include open collectors for stereo and PLL lock indicators, VCO control voltage for tuning meters and envelope-detector automatic gain control of preceding IF and RF amplifiers.

The chip's basic demodulator functions comprise a Type 2 PLL for carrier recovery, I and Q demodulators, a pilot-detection circuit and a sum-and-difference audio matrix. Supporting functions include a dual-bandwidth loop with phase/frequency detector (for mechanically tuned radios), automatic switching between envelope and synchronous detectors (to avoid audio beat notes) and automatic stereo/mono switching.

When used in a frequency-synthesized radio design, the VCO

A dissenting opinion

Thanks to the FCC, the entire AM-stereo scene remains muddled. The benefits of AM stereo (greater geographic range and less multipath distortion) definitely provide a clear advantage over FM. And AM stereo will not significantly increase the cost of existing AM/FM stereo receivers. In addition, the public, particularly people living in areas where FM-stereo reception is more problem than pleasure, will probably accept AM stereo instantly.

What clouds the issue is the time frame. The industry is ready to go, but it's going in different directions. In this respect, the FCC is clearly to blame, say all concerned.

FCC Commissioner Abbott Washburn, following the agency's March 1982 marketplace decision, said it all in his dissenting statement before the panel.

"I submit that this type of marketplace referendum is not the way to make an informed choice, if indeed it results in a choice at all....The data before us shows the performance characteristics of the five systems are so close that consumers of AM stereo will be able to detect little if any difference among the systems....Therefore, whichever system or systems evolve will be based not on true consumer preference resulting from comparison of the five systems, but rather on the size of promotion and merchandising expenditures and like factors.

"It is a proper function of government to lay down the guidelines for a single system that will result in AM stereo in every home at the lowest cost consistent with technical excellence and quality reception....The risk in selecting a single system pales in comparison to the consequence of compelling multiple systems to fight it out in the marketplace....The authorization of a single system will prevent needless delays and avoid the very significant waste of resources by broadcasters, manufacturers and consumers associated with marketplace determination....

"The data and analysis we need to set a standard in AM stereo are before us. I dissent to the majority's unwillingness to make the choice which would have assured a national standard."

For more information...

For more information on the AM-stereo systems and ICs described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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is operated as a buffer, accepting a 4×IF signal from the radio timebase. The PLL loop-filter output is available for application to a voltage-controlled-crystal-oscillator radio timebase.

The HS-3604 specs envelope-detector THD of 0.5% max, which drops to 0.3% for the synchronous detector. Stereo THD is typically 0.3%; separation equals 40 dB. The device operates from 7.5 to 18V dc.

Harris's project engineer for AM stereo, Frank Peters, terms the bipolar HS-3604 a transitional design. He believes that within 1 yr, a less costly implementation will be accomplished via a linear CMOS switched-capacitor filter (SCF).

Peters also acknowledges that a second chip is now in design. Although not expected to be an SCF implementation, it will be an improved version of the HS-3604. But because the HS-3604 is by design totally compatible with Harris's AM-stereo broadcast system, don't be surprised if the second-generation part works with other systems as well.

One chip for all

Meanwhile, Sony and Panasonic, two of the largest receiver manufacturers in the world, could stand to lose quite a lot if they back the wrong system. So both have developed chips to work with more than one of the proposed systems.

According to Keizo Tsukada, staff engineer at Sony's US Consumer Audio Dept, his firm's device can decode all but the Belar AM-stereo signal. The 18-pin bipolar part includes the PLL and detectors required for demodulation. But it requires additional external devices for functions such as pilot-tone detection and phase shifting.

Although this part is being readied for mass production, Tsukada says that a more dedicated chip might be designed if one of the proposed systems gets accepted as a de facto standard. However, he also comments that the cost of the additional components needed to tailor the present system is not great. And even if a de facto standard is adopted, Tsukada says it will take a year before AM-stereo receivers reach the market. So the Sony approach makes market sense.

Panasonic seems to have the same idea. Although few details are available, the company has apparently designed a 3-chip set, combinations of which can be used to decode signals from the various AM-stereo systems. Neither company has any current plans to sell its chips for outside use.

True universal chip?

But what about a single chip that can automatically identify a signal from a particular AM-stereo system and decode it appropriately? Although this might sound desirable, in reality it doesn't make much sense: Such a device's complexity and higher cost would far outweigh its benefits. Therefore, none of the IC companies that have not so far announced AM-stereo designs has any plans to produce such a chip.

In fact, not too many other firms have any plans at all regarding AM stereo. Why? Those that didn't jump into the AM-stereo ring early in the game are not about to make any decision about the technology without confident knowledge regarding the eventual standard. **EDN**

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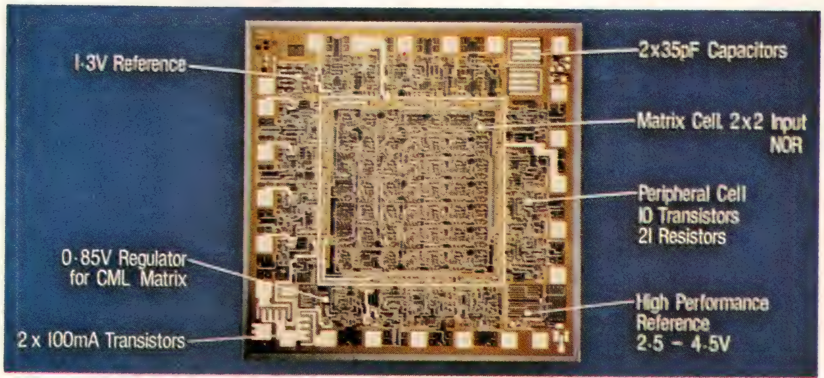

Composed of matrix and peripheral component cells, *Digilin array chips operate from supply voltages of 1 to 5.5V and perform analog, digital and interfacing functions.*

Bipolar Digilin array ICs include multiple cells containing uncommitted active and passive components. They feature high-gain, low-current, single- and dual-emitter npn transistors, as well as shaping capacitors and diffused and pinch resistors with values of 100Ω to 1 MΩ. In addition, the chips include predefined support functions such as bandgap references and series and shunt voltage regulators that permit operation from 1 to 5.5V supplies.

The Digilin Series comprises four array families with complexity ranging from 356 active and 531 passive to 1644 active and 2660 passive components. Each chip includes an array of matrix cells, which perform major circuit functions, surrounded by a ring of peripheral cells that provide user-definable I/O characteristics. Depending on array type and power consumption, maximum clock ranges from 250 kHz to 10 MHz.

The smallest Digilin array, the 100-major-cell ULA1000, comes in three versions. The standard chip typically dissipates 250 mW when fully utilized and operates at 3 MHz max. The ULA1L000, a low-power version, operates at 250 kHz max and consumes 25 mW typ. And a high-speed LSTTL-compatible version, the ULA1H000, operates at 10 MHz max and requires 330 mW typ.

Each of these arrays' matrix cells contains three transistors and five resistors, and each chip provides 28 peripheral cells that include three dual-emitter transistors, seven resistors and a bonding pad. Single matrix cells form 2-input NAND, 3-input NOR and 2-input XOR gates; multiple cells combine to form more complex logic functions.

Larger arrays, the ULA1U000, ULA2U000 and ULA3U000, contain 143, 256 and 280 matrix cells as well as 26, 40 and 48 peripheral cells, respectively. These arrays' matrix cells, optimized for nonsaturated current-mode digital circuits, each contain four transistors and a dual current source. The peripheral cells perform the chips' analog and interface functions.

Typical gate-delay/power product for the U-type arrays equals 1.5 pJ, resulting in propagation time of 450 nsec with low-power gate designs and 150 nsec with triple-power circuits. Maximum clock rate varies from 440 kHz for single-power gates to 1.3 MHz for higher power switches. Each of the U-type arrays' matrix cells forms two 2-input NOR gates or one 4-input circuit, and you can wire-OR gate outputs to form more complex circuits.

You can design and lay out Digilin arrays yourself using a CAD system or a set of Mylar-film-based manual tools. Alternatively, the manufacturer can design arrays using your schematic drawings.

To simplify the layout of multiple circuits, the firm offers its $100,000 ULA designer workstation, a dedicated CAD system that supports layout as well as circuit simulation and test-schedule verification. For analog-circuit breadboarding, the firm provides a set of packaged linear-array components, and you can request SPICE modeling of analog designs before chip fabrication.

Typical Digilin development costs range from $8000 to $40,000, depending on production commitment and level of interface with the manufacturer. Production chips cost $5 to $14 (10,000). Delivery of engineering samples, 8 to 20 wks; production shipments begin 10 wks after prototype approval.

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CIRCLE NO 34

Editor's Choice: New Products

Low-cost programmable plug-in module adds digital power to scope family

A programmable plug-in, *Model 7D20 adds low-cost digital power to its manufacturer's 7000 Series scope mainframe.*

The $7750 7D20 plug-in converts its manufacturer's 7000 Series mainframe into a powerful digital scope. It features capabilities such as pretrigger information capture, signal averaging, GPIB programmability, waveform storage, Roll mode, real- or equivalent-time sampling and dual-channel acquisition at full sample rate and resolution.

The 7D20 samples at 40 MHz, thus providing a 10-MHz stored-information bandwidth in the real-time sampling mode and a 70-MHz capture bandwidth for repetitive signals in the equivalent-time sampling mode. An efficient acquisition algorithm minimizes the number of sweeps required to capture a waveform in the equivalent-time mode.

Bidirectional bus

You can program the plug-in over the GPIB interface in a language that's familiar to scope users. The digitized information can be transmitted back through the GPIB; thus, you can use the plug-in as a source in a data-acquisition system.

You can also program several 7D20 controls as interrupts to the GPIB controller for use as soft keys, permitting branching to a different control program. This feature proves useful in diagnostic operations—it lets an inexperienced user follow a diagnostic tree programmed into the controller. You can store six front-panel setups in an EAROM and recall them from the front panel.

Other features that enhance instrument flexibility include the Roll mode (with a 0.1- to 20-sec/div setting range), which optimizes the viewing of slowly changing events. And the instrument's enveloping feature sets limits for measurements or reveals subtle variations in repetitive signals.

Several averaging modes let you recover signals buried in noise. And the cursor readout allows single-point or point-to-point measurements of both time and amplitude.

Friendly, menu-driven software completes the package with extensive diagnostic and self-check features. Alphanumeric readouts are available for all screen parameters, including cursor measurements, waveform scale factors, waveform ID, prompting and menus.

Tektronix Inc, Box 500, Beaverton, OR 97077. Phone (503) 644-0161.

Circle No 452

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Hitachi's New EPROM-based Microcomputers Solve the Problems of Mask-programmed MCUs.

- No mask charge . . . they're programmable at your factory or by your field personnel
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- No special programming equipment required . . . Hitachi's "piggyback" approach utilizes industry-standard EPROMs and programming equipment
- No technology constraints . . . innovative packaging approach allows EPROM content from 16K to 64K for the HD68P01, and 32K for the HD68P05

Features of the Hitachi HD68P01

- Emulates both 2K byte (HD6801S) and 4K byte (HD6801V) mask-programmable MCUs
- Expanded HMCS6800 instruction set
- 8 x 8 multiply instruction
- Serial communications interface (SCI)
- Upward source and object code compatible with HD6800
- 16-bit three-function programmable timer
- Accepts industry-standard EPROMs:
  - 2K x 8 HN462716
  - 4K x 8 HN462732 or HN462532
  - 8K x 8 HN482764
- 128 bytes of RAM (64 bytes retainable on powerdown)
- 29 parallel I/O and two handshake control lines
- Internal clock generator with divide-by-four output
- Single-chip, or expandable to 65K bytes of external memory
- Bus compatible with HMCS6800 family

Features of the Hitachi HD68P05

- Emulates all HD6805 mask-programmable MCUs (1K, 2K, and 4K byte versions)
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- Memory mapped I/O
- Internal 8-bit timer with 7-bit prescaler
- 24 I/O ports + 8 input ports
- Accepts industry-standard EPROMs:
  - 4K x 8 HN462732 or HN462532
- On-chip clock circuit
- Master reset
- Byte efficient instruction set
- True bit manipulation
- Bit test and branch instructions
- Powerful indexed addressing
- Full set of conditional branches
- Memory usable as registers/flags
- Single instruction memory examine/change
- 10 powerful addressing modes
- All addressing modes apply to ROM, RAM and I/O
- Compatible instruction set with HD6805

If you'd like to say "Yes" to Hitachi's HD68P01 and HD68P05 piggyback EPROM/MCU devices, return coupon or call your local Hitachi Representative or distributor sales office for more information.

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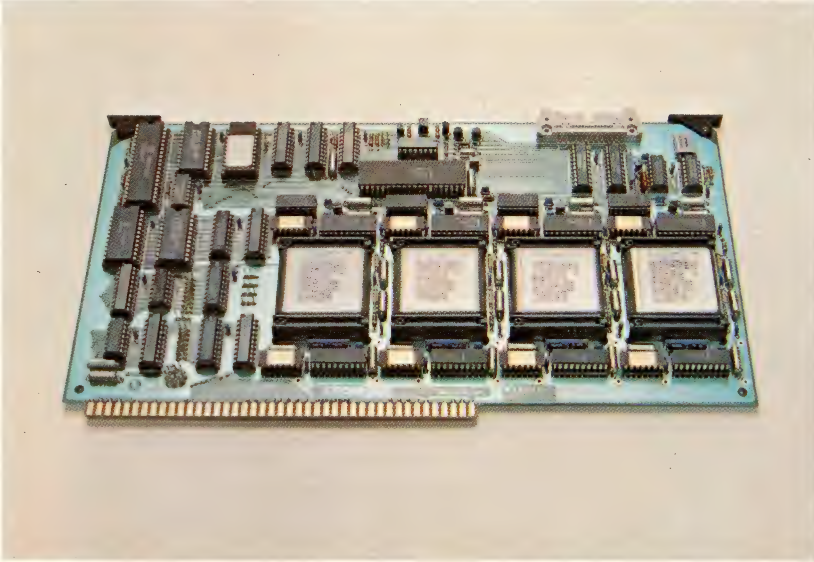
EDN92982-111

Editor's Choice: New Products

Multibus-system bubble-memory card accommodates harsh environments

Combining an intelligent controller and 512k bytes max of bubble memory on one Multibus-compatible card, the MBI-1 bubble-memory system provides reliable mass storage for Multibus-based μC systems. It can operate in harsh environments where dust, smoke, vibration, shock and high operating temperatures preclude the use of electromechanical mass-storage devices. The board operates over 0 to 70°C and loses no data over a −40 to +100°C storage range.

A Z80-μP-based controller handles all memory housekeeping chores—it takes care of memory formatting, control and interfacing. And the same controller can handle as many as 8M bytes of bubble memory on expansion boards.



Aimed at use in harsh environments, *the MBI-1 serves as a controller and furnishes as much as 512k bytes of bubble memory for a Multibus system.*

Talking and remembering

The host computer transfers data to and from bubble storage in blocks, using a high-level command set. A 14-bit Fire code detects errors (the MBI-1 can correct bursts five bits long).

Additional commands let the host initiate a set of diagnostics that verify the system's operation. The bubble-memory controller keeps a log of all errors (ERRLOG); the log is available on command.

The bubble controller runs under CP/M and executes CP/M directly from bubble memory. The MBI-1 operates more rapidly than a floppy disk, achieving access time to first data byte of less than 41 msec avg.

You can transfer data to and from bubble storage at more than 270k bps. You read and write the data in multibyte blocks, programming the controller for 64-, 128- or 256-byte block sizes.

The 512k-byte MBI-1 requires 5V at 0.9A and 12V at 0.1A when in standby and 1.2A when shifting bubbles. Smaller capacity boards use less power.

128k bytes, $947; 512k bytes, $2247 (100). Either board comes with sample software drivers written in both Z80 and 8085 assembly language. CP/M, $400.

Bubbl-Tec, 6800 Sierra Ct, Dublin, CA 94568. Phone (415) 829-8700.

Circle No 451

NEXT TIME

EDN's October 13 issue will feature a Special Report on capacitors. Also look for design features on

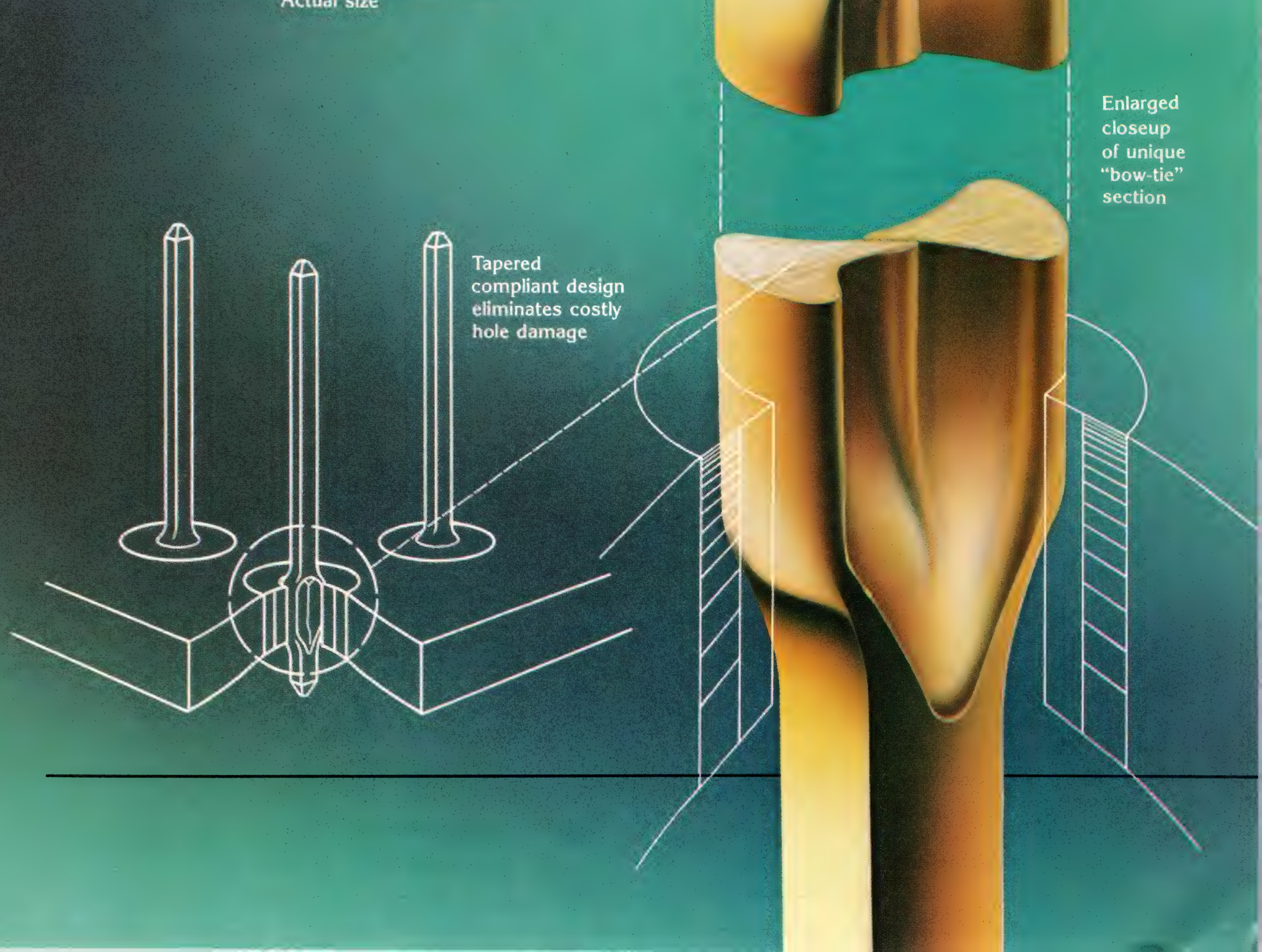
- How to deal with capacitor dielectric absorption (soakage)
- How to select the Winchester disk drive that best suits your application

Leading off the issue will be a Technology Update on optoelectronic ICs. And you won't want to miss our regular Design Ideas department, either.

EDN: Everything Designers Need

Berg Press-Fit Pin: complies with wide hole

Actual size



holds fast without solder, tolerances and tight budgets

Berg's new compliant Press-Fit pin delivers high retention forces without solder or costly hole damage. Press-Fit is tested for an average of 16 lbs. in the largest hole size, assuring electrical and mechanical integrity. It accommodates a variety of board thicknesses and a wide range of plated-through holes, reducing the need for more tightly controlled board manufacturing procedures. And it's backed with the widest choice of application equipment available. The result: reliable connections at low applied costs.

mass insertion or fully automatic machine insertion, with speeds up to 15,000 per hour. The pin is available in an assortment of above and below board lengths.

Edge card connector terminals are also available with the "bow-tie" press-fit section. These terminals incorporate two-point, pre-loaded support springs to provide higher normal force and lower insertion force than cantilever springs. Both pins

"Bow-Tie" section (enlarged) before insertion

From 0.043″ to 0.035″, a tight grip with a gas-tight fit and no solder

The Berg Press-Fit pin features a unique "bow-tie" press-fit section. This section yields in shape to form a gas-tight connection with holes from 0.043″ (1.09mm) to 0.035″ (0.89mm) and ensures high retention forces. Even after repeated replacement, the pin maintains a retention force well above the industry requirement of 10 lbs.

Berg's Press-Fit pins, either stamped or drawn wire, are supplied in strip form to allow manual

and terminals are available in a number of gold or tin platings.

There's no need to risk solder contamination, with accompanying corrosion or thermal shock, any longer. Specify the Berg Press-Fit pin or edge card terminal and reduce your manufacturing costs. Call toll-free 800-233-1450 (PA residents: 717-975-2000), or write for bulletin 7000. Berg Electronics, The Du Pont Company, Camp Hill, PA 17011.

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CIRCLE NO 36

Leadtime Index

ACTIVE COMPONENTS

PRODUCT	LEADTIME IN WEEKS Min.	Max.	Trend
DISCRETE SEMICONDUCTORS			
Diode, switching	2	4	=
Diode, zener	2	8	=
Rectifier, low-power	2	5	=
Rectifier, power	4	8	=
Thyristor, low-power	5	15	⇧
Thyristor, power	4	18	⬇
Transistor, bipolar power	2	8	=
Transistor, bipolar signal	2	12	=
FET, power	4	7	=
FET, signal	3	7	=
Transistor, RF power	4	13	⬇
DISPLAYS			
Fluorescent	3	12	=
Gas-discharge	5	10	=
Incandescent	8	18	=
LED	4	16	=
Liquid crystal	3	9	⇧
Plasma panel	6	15	=
ELECTRON TUBES			
CRT, black and white TV	10	14	=
CRT, color TV	2	8	=
CRT, industrial	4	15	=
Industrial power	4	11	=
Light and image sensing	2	10	=
Microwave power	7	10	=
INTEGRATED CIRCUITS, DIGITAL			
CMOS	4	15	⇧
Diode transistor logic (DTL)	5	10	=
Emitter-coupled logic (ECL)	4	8	=
Low power Schottky TTL	2	14	=
Standard Schottky TTL	7	14	⇧
Standard TTL	2	8	=
INTEGRATED CIRCUITS, LINEAR			
Communications circuit	3	6	=
Data converter	2	6	=
Interface circuit	2	6	=
Operational amplifier	4	12	⇧
Voltage regulator	4	13	⇧

PRODUCT	LEADTIME IN WEEKS Min.	Max.	Trend
MEMORY CIRCUITS			
EPROM	2	10	=
PROM, bipolar	5	12	=
RAM, bipolar	4	20	=
RAM, CMOS	2	10	=
RAM, 4k MOS dynamic	4	8	=
RAM, 16k MOS dynamic	4	10	⇧
RAM, 64k MOS dynamic	6	22	=
RAM, 1k MOS static	4	8	=
RAM, 4k MOS static	4	10	=
ROM, masked MOS	3	12	=
MICROCOMPUTER/MEMORY SYSTEMS			
Core memory board	3	10	=
IC memory board	4	8	=
Interface board	6	8	=
Microcomputer board	6	14	=
MICROPROCESSOR IC'S			
CPU, bipolar bit slice	3	4	=
CPU, 4-bit MOS	2	4	=
CPU, 8-bit MOS	4	6	=
CPU, 16-bit MOS	4	12	=
Peripheral chip	2	10	=
OPTOELECTRONIC DEVICES			
Coupler and isolator	4	8	=
Discrete light-emitting diode	5	12	=
PACKAGED FUNCTIONS			
Amplifier, instrumentation	6	12	=
Amplifier, operational	6	12	=
Amplifier, sample/hold	4	8	=
Converter, analog/digital	2	6	=
Converter, digital/analog	2	6	=
PANEL METERS			
Analog	4	10	=
Digital	4	8	=
POWER SUPPLIES			
Custom	18	30	=
Enclosed modular	6	12	=
Open-frame module	10	15	=
Printed circuit	9	15	⇧

Leadtimes are based on recent figures supplied to *Electronic Business* magazine by a composite group of major manufacturers and OEMs. They represent the typical times necessary to allocate manufacturing capacity to build and ship a medium-sized order for a moderately popular item. Trends represent changes expected for next month.


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CIRCLE NO 37

THE CURIOUS INCIDENT OF THE 9-BIT 8-BIT DAC

"Just think, Watson," said Sherlock Holmes as they shared a pot of tea in their suite at the Barbizon-Plaza Hotel and watched the sun set over Central Park, "it may only have been PMI's DAC-208/210 D/A converters that saved Alec Cunningham's life."

The curious incident had begun only that afternoon as the famous detective and his friend stepped outside of the New York Coliseum for a breath of fresh air. "Last time I'll accept your invitation to take in a show in New York," Dr. Watson was complaining about the trade show. "Industrial controls, indeed! I expected *A Chorus Line* and you show me assembly lines."

Holmes was distracted by a familiar face in the crowd, that of Alec Cunningham, president of Opni Systems and one of Silicon Valley's brightest entrepreneurs. Cunningham hailed a cab and told the driver, "Empire State Building."

"Strange," said Watson. "Time for sightseeing in the midst of a trade show?"

"Too strange," Holmes answered as he turned quickly back into the Coliseum.

At the Opni booth, the mystery began to unravel as the firm's sales manager spoke. "I'm worried too, Mr. Holmes. Alec began acting strangely today when a competitor, Gaben Data, announced a data acquisition system for industrial control similar to the one he's been working on. Only Gaben's is faster, cheaper, and more accurate."

"A real triple threat," said Holmes. "And yet we've used the fastest microprocessor available anywhere," the sales manager continued.

Holmes reflected for a moment. "But I thought that most problems with microprocessors in industrial controls stem from the analog-to-digital and digital-to-analog conversion interfaces."

"Quite right, Holmes," the man continued. "But we spared no expense to buy the best hybrid DACs available, with the reference and op amp designed right into the package."

Curiosity sparkled in Holmes' eyes. *Why pay all that money for hybrids,* he wondered, *when there must be a monolithic DAC that would do it better at lower cost?*

"We haven't a moment to lose," Holmes said to Watson. "No questions—just dash back to the hotel and get the monolithic DAC file from my valise. Then get a cab back here and keep it waiting out front."

A short time later he jumped into the cab and instructed the driver,

"Don't do anything hasty," Holmes said before he began telling Cunningham how the DAC-208/210 could solve the design problems of his data acquisition system.

"Empire State Building, and step on it. A man's life may depend on it!"

Holmes wasted no time telling Watson how he had been shunted aside by Gaben's booth personnel. "Clearly, I was not perceived to be a Qualified Lead. But I picked up what may be a clue—'sign-magnitude coding'. I also heard a discussion of 9-bit DACs, which puzzled me. Let's begin the search."

As the cab bounced down Seventh Avenue towards 34th Street, Holmes instructed Watson to help him read DAC data sheets, beginning with PMI. "After all, they *invented* monolithic DACs in 1970 and their DAC-08 has been the industry standard since they introduced it in 1974."

Watson had just begun to shuffle through the papers when Holmes exulted, "Here it is!," as he scanned the DAC-208/210 literature. "Sign-magnitude coding! It evidently eliminates many of the problems of Offset Binary coding and Two's Complement coding, including non-symmetrical output and the current-carry errors at analog zero, the very place where the greatest accuracy is required. In sign-magnitude coding, the output is divided into positive and negative outputs, which are *symmetrical* around zero."

"But those are 8-bit and 10-bit DACs," Watson interrupted. "You said *nine* bits."

"Ahh, but listen," Holmes continued. "A sign-magnitude coded DAC has an extra bit of resolution—the sign bit. Thus in the 8-bit DAC-208, there are 9 bits of resolution; in the DAC-210, there are 11. Don't you see, Watson, in Offset Binary or Two's complement you must use the Most Significant Bit for the sign bit. A sign-magnitude coded DAC lets you reverse polarity on the output signal—in essence giving you an extra bit."

The cab screeched to a halt and Holmes quickly led Watson up to the observation deck. They spotted Cunningham, one leg over the guard rail, staring at the street far below.

"Do nothing hasty, my friend," he said, gently taking the man's arm. "I've just found the solution to your problem." Calmly, he began to recap his new-found knowledge to the distraught Cunningham.

"But my hybrid gives me everything in one package," he argued.

"So does PMI's DAC-208, and at a fraction of the cost," Holmes insisted. "It's like having a DAC-08 with an internal reference and output op amp added, *plus* an extra sign bit at no extra cost. And if 9 bits are not enough, the DAC-210 gives you 10 bits plus sign with full-scale symmetry ± 1 LSB."

"But speed and accuracy are really important to me, Holmes," Cunningham said, his interest growing.

"The DAC-208 is the *fastest* complete monolithic DAC on the market. Settling time is 750ns, with a temperature coefficient of 40ppm/°C, which means less than ½ LSB drift over the full 0-70°C range. And for your military marketplace, PMI gives you similar specs in military grades."

Cunningham looked puzzled. "How did you know we plan to enter the military systems market?"

"One picks up all kinds of rumors at trade shows," Holmes smiled.

A short time later, Cunningham was on his way back to California to begin redesign of Opni's new system while Watson and Holmes finished their tea.

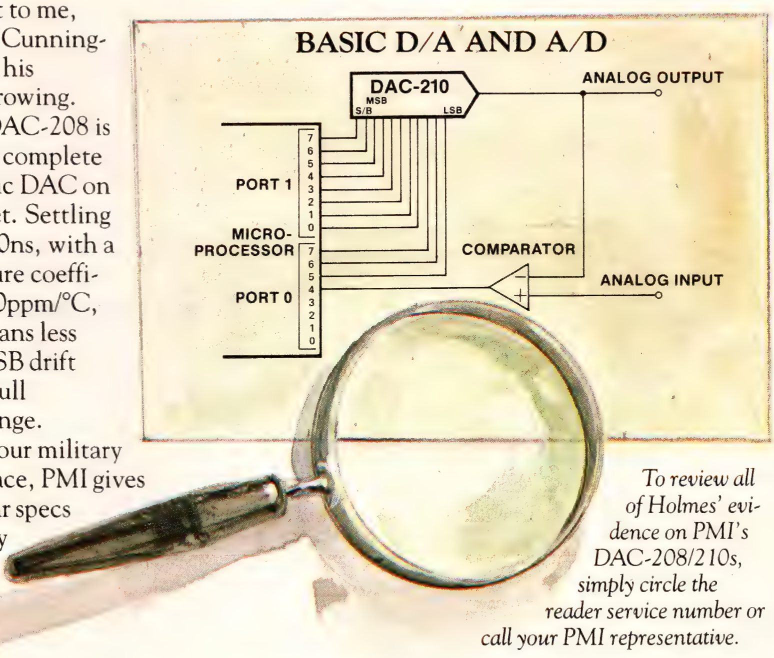
"Well done, Holmes," Watson said. "A busy day indeed."

"Not so busy that I didn't manage to buy theatre tickets, Watson. We can just make the curtain if we rush."

"*A Chorus Line?*" Watson asked hopefully.

"Tenth row center," Holmes assured him.

Watson beamed as he reached for his bowler. "Now *that* is my idea of a Qualified Lead!"



To review all of Holmes' evidence on PMI's DAC-208/210s, simply circle the reader service number or call your PMI representative.

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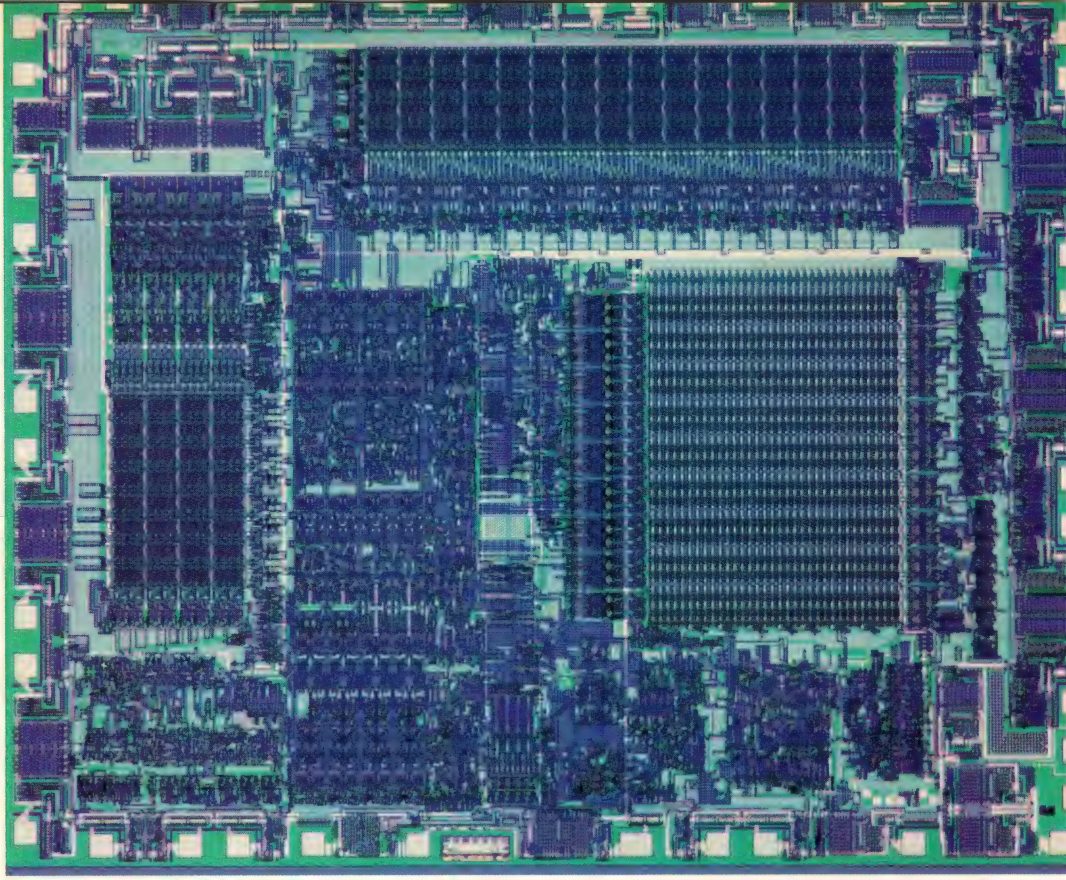
See us at the Bourns GmbH booth at Electronica

CIRCLE NO 200



Can you spot the difference? *The classical-CMOS RCA CDP1805A single-chip μC (left) is fully static, consumes 7.5 mW in operation and 0.25 mW in standby, and operates over −40 to +85°C. The National Semiconductor NSC800 (right), on the other hand, consumes 50 mW in operation and 25 mW in standby and functions over 0 to 70°C. The more complex NSC800 is an example of a growing trend: the selective use of CMOS circuit functions in an otherwise NMOS device. The approach provides both advantages and drawbacks—features with which you must be familiar if you're contemplating a switch to some sort of CMOS solution to a system-design problem. (Photos courtesy RCA)*

CMOS microprocessor and microcomputer ICs

Robert H Cushman, Special Features Editor

Every key 4- and 8-bit μP and single-chip μC now comes in a CMOS version, and 16/32-bit devices will, too. But how does the NMOS/CMOS technology used in some of these parts compare with classical CMOS?

The CMOS bandwagon has begun to roll: Chances are good that within the next few years you'll use a CMOS version of the μP or single-chip μC you now employ. As EDN has reported **(Ref 1),** 30 of the approximately 40 NMOS μP/μC families are either now available in CMOS or soon will be. And because in many cases more than one source is developing a CMOS version of a given μP or μC, hundreds of CMOS device types could soon be in existence.

The appearance of such a large number of CMOS devices might not be so surprising if the trend were confined to the 4- and 8-bit 1-chip μCs, which are aimed at use in battery-operated systems. But the switch to CMOS is also apparent in midrange, multichip 8-bit μPs, the machines that see the broadest, most general-purpose use. And now, with the announcement that National's NS16000 will eventually appear in CMOS, even the new 16/32-bit NMOS machines are represented in the trend.

The trend is so pervasive, in fact, that some industry observers predict that by 1990, CMOS parts will be more available and more standard than NMOS devices. Fortunately, most of the new CMOS parts, including memories and support chips, are being designed as drop-in NMOS replacements.

But the switch to CMOS is not confined to such NMOS replacements. CMOS SSI and MSI gates are also being designed as drop-in replacements for TTL

CMOS finds use across the entire μP/μC spectrum

μP-system glue parts. And in a parallel development, more CMOS gate arrays are appearing, which will allow μP-system designers to develop their own custom CMOS subsystems.

Is it really CMOS?

For more than a decade, CMOS, in the form of SSI and MSI logic gates (from RCA, Motorola, National, Fairchild and other suppliers) has had its staunch admirers, who have asserted that the technology is ideal in all respects except economical VLSI circuitry and speed. If you are among this band of CMOS lovers, you are probably eagerly awaiting the new CMOS μPs and μCs, which promise competitive VLSI circuits and high speed as well. But be warned: These advantages will come at a price. The CMOS being used in these μPs and μCs isn't classical CMOS. Much of it is really NMOS, to which 10 to 40% CMOS has been strategically added.

This approach has both good and bad points. On the plus side, you won't have to pay an all-CMOS price premium for the new μPs and μCs. But on the minus side, the technology's performance might be disappointing if you really are expecting the superlative performance of classical CMOS.

Recall that classical CMOS consists of 50% p devices and 50% n devices, which function in matched pairs to form inverters, transmission gates and other components **(Figs 1 and 2)**. The ideal nature of a classical CMOS inverter's performance arises from the positive, push/pull action of the two enhancement-mode devices, producing a clean, trigger-like switching transfer function (also shown in **Fig 1**). That is, one device goes fully ON while the other goes fully OFF. As a result, the output signal swings solidly from one supply rail to the other, and only miniscule currents flow through the inverter after it has switched—mere nanoamperes. This static dissipation appears in the horizontal part of the familiar dissipation-with-frequency curve, shown in **Fig 3.** It's the reason a CMOS wristwatch, for example, operates for years from a tiny button battery.

Although the basic inverter pair does dissipate power when switching through the active region (in the middle of the transfer graph, **Fig 1b**), the dissipation arises not so much because both transistors are briefly ON, but from the charging and discharging of the

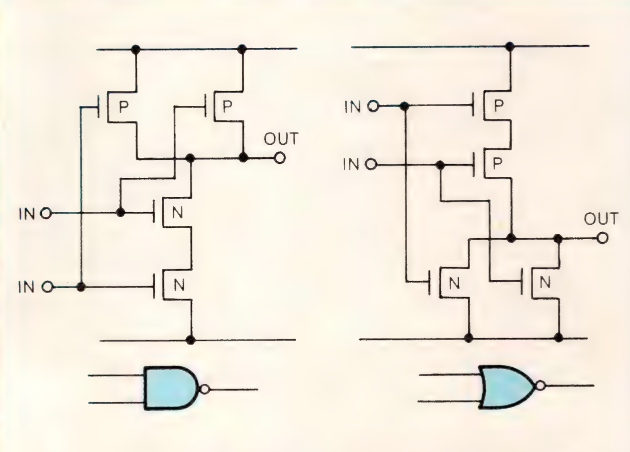


Fig 2—Logic functions *are performed in classical CMOS by combining p and n pairs, as shown for these simple 2-input NOR and NAND gates. A classical-CMOS device maintains a strict 50:50 balance between the number of p and n devices.*

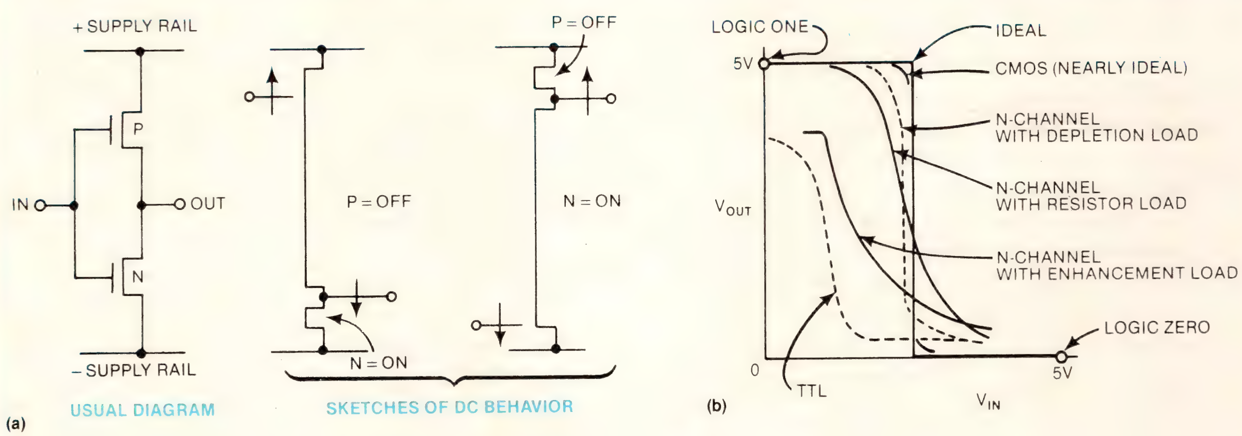
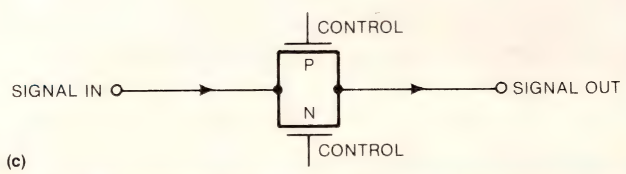


Fig 1—The basic CMOS circuit elements *are the inverter pair* **(a)** *and the transmission gate* **(c)**. *The inverter connects across the supply rails, while the gate is inserted in a signal path as a controllable series impedance. The inverter pair's transfer function* **(b)** *illustrates the ideal performance of CMOS compared with single-channel NMOS or bipolar TTL: Note the rail-to-rail snap action of an ideal CMOS switch.*



circuit capacitance during the switching transition. This dissipation increases with frequency and is graphed in the upward-sloping portion of **Fig 3**'s curve.

Fig 3 is fundamental to an understanding of CMOS's low-power advantage. It tells you at a glance that CMOS is no better than any other technology when operating at megahertz clock speeds; you can only gain the CMOS low-power advantage when you can slow down a CMOS part's gates—either by reducing the clock frequency or by turning the clock on and off for intermittent duty cycles. If the CMOS chip is designed so that as few of the gates as possible must run at full clock speed, so much the better.

But another problem—beyond the gate-level considerations—makes it impractical to fully convert an NMOS μP or μC system to CMOS. Such a system is necessarily built around large amounts of memory, and the central arrays of such memory can only be economically produced with single-channel circuitry. Most chip designers agree that adding extra p devices in the central arrays of ROMs and EPROMs would be unthinkable—and unnecessary, because these arrays can consume little power if only activated when read.

Adding p-channel devices to RAMs makes more sense, if the RAMs aren't too large, but even here chip designers make compromises. As shown in **Fig 4**, if they do use a full-CMOS flip flop, they nevertheless employ single-channel transmission gates to drive it. More likely, they use very-high-resistance polysilicon load resistors in place of the p-channel devices in the flip flop; the poly loads provide the static circuit behavior expected with classical CMOS but allow for a more compact, single-channel central array.

The fact of the matter, then, is that most of the "new CMOS" is just the same old NMOS, to which chip designers have added a touch of CMOS. It's being produced on what are essentially NMOS processing lines: Adding the p-channel circuitry isn't difficult, because NMOS processes have grown to so many steps—11 or so—that the additional few steps required for p devices aren't significant, especially with the modern n-well approach.

Where is CMOS used?

Now that chip designers do have the freedom to add p-channel circuitry and create CMOS stages, how do they use this new freedom? Everywhere but in the larger memory-cell arrays (**Fig 5**). Specifically, the circuitry appears in decoders, drivers and sense amplifiers around the memory arrays and in all of a μP's random-logic areas, such as the ALU and clock drivers. In addition, it's used in off-chip interfaces.

How much CMOS appears on a chip appears to depend on the designers' goals. According to Richard Ahrons of RCA, the three classes of currently available

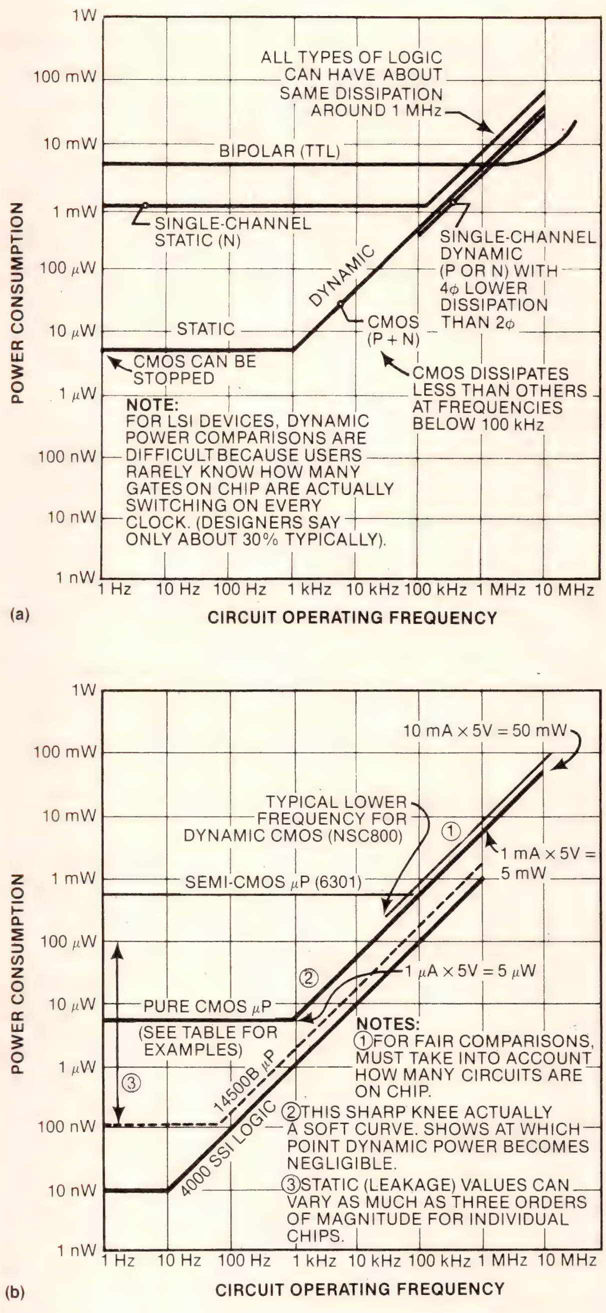


Fig 3—A power-consumption-vs-switching-frequency curve (a) *is the key to understanding how to take advantage of CMOS. All digital gates are subject to the same two types of dissipation—static and dynamic. However, the static dissipation of most is so high that they continue to consume the same large amount of power even when their switching rates are reduced. CMOS, on the other hand, specs such a low static dissipation that its total power consumption drops as the clock rate decreases. Dynamic single-channel NMOS (and particularly 4-phase logic) has much the same characteristics as CMOS, but because it's dynamic, the clock can't be slowed beyond a certain point, particularly at higher temperatures. Representative power-speed levels appear for several CMOS devices in* **(b).**

Quasi-CMOS has high speed, but at a price

CMOS can be defined by the degree to which p devices are added:

- Classical CMOS, where the chip designer strives for a 50:50 p-to-n ratio. This approach is the most expensive in terms of chip area but is used when the ultimate in CMOS performance is required. It might serve, for example, in systems that must operate for long periods from small batteries or at extreme temperatures (for instance, down-hole instrumentation in oil-well drills, which must survive at temperatures to 200°C). It also serves in radiation-hardened equipment, although silicon-on-sapphire (SOS) devices might also be used in this case.
- Commercial CMOS for midrange systems, where the chip designer wants to strike an economical tradeoff between moderate chip-size increase and increased CMOS performance. Here, 40:60 to 20:80 p-to-n ratios might serve. Most of the CMOS versions of 8-bit μPs fall in this category.
- Specialized CMOS, used in devices where the chip designer normally would remain with NMOS but must deal with circuit hot spots. In such cases, the designer could selectively throw in a relatively small number of p devices to meet certain design goals, such as use of a lower cost plastic package or the ability to operate at a higher temperature. CMOS might function on this basis in the advanced, very dense VLSI chips for 16/32-bit μPs and their support circuits.

How do the CMOS chips stack up?

Having reviewed the basics, consider some representative examples of CMOS μPs and single-chip μCs. The nearby **table** lists these devices; keep in mind, though, that they're a small number of the hundreds of CMOS chips that are becoming available.

The **table** contains columns for checking off whether the devices listed have certain features of interest in CMOS applications. They represent some of the questions you should be asking, such as:

- Can the part operate over the full −55 to +125°C military range? Classical CMOS can, with ease.
- Can the clock go down to dc? Classical CMOS can—CMOS is inherently static.
- Does the part have microwatt-level standby power? Classical CMOS does, when the clock is stopped or less than 1 kHz.

The case for CMOS

Garry J Anderson,
Baradine Products Ltd

Three problems exist in systems utilizing TTL and NMOS parts: poor electrical noise immunity, narrow operating-temperature range and excessive power-supply requirements. CMOS overcomes all of these problems.

The case for CMOS is best argued in terms of the many and varied application areas that benefit from using it. The technology is most valuable in industry; most industrial sites have problems with electrical noise, and some exhibit wide temperature fluctuations. In addition, some undergo frequent power outages. In these applications, a CMOS system, with its higher noise immunity and wider temperature range and adaptability to battery backup, is superior.

In addition, remote data-acquisition systems are often battery powered and operate in an outdoor temperature environment. Here, CMOS's low power and wide temperature range are essential.

But CMOS also has virtues of great interest to nonindustrial users. For example, quiet zones such as hospitals and offices can't tolerate the constant, irritating noise of a cooling fan and hence require fanless, convection-cooled systems. At the same time, the personal computers and terminals that are proliferating in these user environments are being installed with larger and more tightly packed memory boards. With current NMOS, these closely spaced memory boards demand cooling fans. But switching to CMOS in these systems eliminates the need for fans and, in addition, provides the desirable feature of battery backup.

The case for CMOS can be further argued in terms of the general trend toward smaller, lighter, more trouble-free systems in all application areas. Using the technology allows you to halve system size and weight.

For example, in an NMOS-plus-TTL system, a linear-regulated power supply occupies as much of the total volume as the system board—50%. In a CMOS system, however, the power supply only occupies 10% of the total volume. In addition, you can eliminate cooling fans and their associated enclosure openings and dust filters. The resulting CMOS system is thus smaller, lighter and more reliable. It can in addition be sealed against dust and customer-personnel prying and thus be much more likely to operate maintenance-free for years.

Garry J Anderson *is president of the North Vancouver, British Columbia manufacturer of CMOS board-level products.*

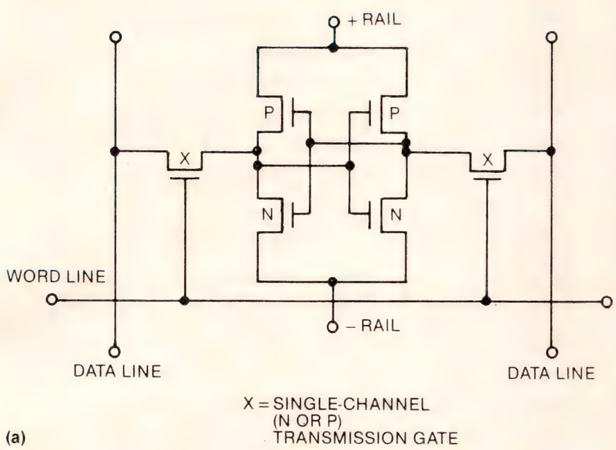


Fig 4—Even in classical CMOS, *RAM cells are rarely all CMOS* ***(a).*** *Although they have fully CMOS flip flops, the transmission gates for accessing those flip flops are invariably just single-channel NMOS. Often, to further keep memory-cell size small, manufacturers substitute polysilicon load resistors for the p devices in the flip flops* ***(b).*** *Such poly loads keep the RAM static, and they can spec very high resistance (many hundreds of megohms), so static power drain is no more than that of pure CMOS. Unfortunately, these devices might be unstable at high temperatures.*

Such insight into the nature of a device's CMOS circuitry could work for you in two ways. If your application calls for the ultimate in low power, you'll want to choose devices that are close to classical CMOS, regardless of their chip size. But if your design will always be running at megahertz clock rates and you want minimum cost, you'll want to choose a compromise "semi-CMOS" part.

The 1-bit Motorola MC14500B (**Ref 2**) appears in the **table** because it's probably the only μP that is fully classical CMOS. It was introduced in 1977 as part of the Motorola B Series CMOS logic family and accordingly is fully static (consuming only 5 nA in the quiescent state) and operates over the full military temperature range (in a ceramic package, of course). Like the B Series devices, it can operate from supply voltages between 3 and 18V, which gives it an edge in high-noise-immunity systems and systems operated directly from unregulated power sources.

The MC14500B comes in a 16-pin package and is fairly fast (1 μsec) at performing bitwise decision tasks. Motorola's David Babin, who has been handling applications for the device, says customers are using it with other B Series CMOS logic to implement relay-ladder logic and programmable controllers. The only catch for the purist is that there are no ROMs in the B Series. True, currently available CMOS ROMs and EPROMs spec adequately low power consumption and withstand military-level temperatures, but none of them operate to 18V. Thus, you must resort to such dodges as transferring the program from a ROM or EPROM into some of the small B Series RAMs (like the 64×4 14552) upon system startup.

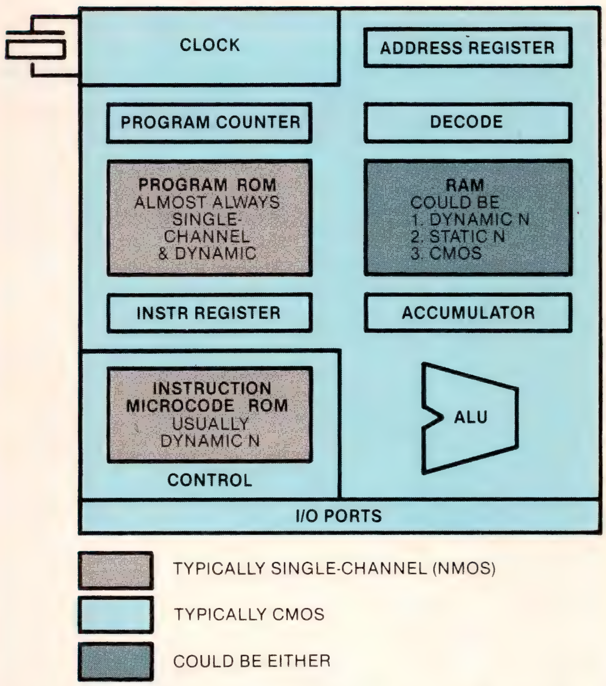


Fig 5—NMOS areas on a quasi-CMOS chip *include the central arrays of the program ROM, the microinstruction ROM and sometimes the RAM. In most cases, the arrays used in ROMs (and in many EPROMs) are dynamic as well as single channel. But this construction should not interfere with clock shutdown because the ROMs are of course nonvolatile. The RAM, however, had better not be dynamic if the part is to be put to sleep and reawakened. Much advantage still accrues to fabricating the rest of the chip in CMOS: the clocking, memory-address decoders, control, ALU and I/O are usually where most chip power is consumed anyway.*

No μP/μC system can be fully converted to CMOS

This lack of B Series memories, plus the 14500B's primitive architecture (only 16 instructions and no program counter), raises questions about the device's ultimate appeal. At least one Motorola spokesman agrees that the firm's 146805 single-chip μC would be a better choice. An interesting arrangement might be to have the 14500B serve as a peripheral to a μC like the 146805, with that μC feeding the instructions to the 14500B. Because the 14500B is static, these instructions could be fed asynchronously, as needed.

The Sharp 530 and 531 4-bit single-chip CMOS μCs appear in the **table** because they epitomize the type of CMOS that has permitted the proliferation of some rather remarkable consumer products—thin-line pocket calculators and multifunction wristwatches. Most consumers now take the prices and performance of these CMOS-based products for granted. Yet designers should consider what these qualities could mean to their product designs, now that CMOS building blocks are becoming more generally available.

The 530 and 531 operate from single 1.5V cells and spec power dissipation of only 12 μA at watch-crystal clock frequencies (32.768 kHz) and only 1.5 μA in Standby mode. This class of μC is intended as a complete 1-chip solution for lowest cost consumer products, so in the future it will typically include a growing number of additional functions. For example, the two Sharp devices include their own LCD drivers and melody-generating circuits.

To service all the 530/531's inputs and outputs yet be able to use a small package, Sharp has chosen a ½-in.-square flatpack with 60 leads distributed on all four sides. These miniaturized packages should gradually become more widely used with CMOS devices as designers find they can squeeze more circuits closer together and still not require external cooling.

The 4-bit National COP, 8-bit Motorola 146805 and 8-bit NEC 80C48 appear in the **table** as good examples of low-end CMOS building blocks for μP-based systems. Although mainly intended as masked-ROM high-volume

REPRESENTATIVE CMOS μPs AND μCs

DEVICE	SUPPLIER(S)	DESCRIPTION
MC14500B	MOTOROLA	PRIMITIVE 1-BIT PROCESSOR TO BE USED WITH SSI AND MSI CMOS LOGIC GATES.
SM-530 SM-531	SHARP	HIGH-VOLUME 4-BIT DEVICES FOR MINIATURE, BATTERY-OPERATED PRODUCTS. SUPPLIER HAS FOR SEVERAL YEARS DEMONSTRATED THAT THESE μCs CAN BE SOLD INTO COST-COMPETITIVE CONSUMER APPLICATIONS.
COP	NATIONAL	FLEXIBLE 4-BIT CONTROLLER FAMILY, WITH WIDE VARIETY OF BUILDING-BLOCK PARTS. GOOD POWER-DOWN OPERATION.
MC146805(E2) 146805(G2) (ROMless & ROM)	MOTOROLA (RCA)	8-BIT μP/μC WITH EXCELLENT ASLEEP/AWAKE CONTROLS. IS FINDING ACCEPTANCE IN BATTERY-POWERED INSTRUMENTATION. ENTIRE CPU BOARD BASED ON PART (FROM SYNAPSE) ONLY CONSUMES 20 mA RUNNING AND 50 μA STOPPED.
80C48 (80C51 TO FOLLOW)	NEC (NATIONAL, INTEL, & MANY OTHERS)	CMOS VERSION OF INTEL'S WIDELY USED 8-BIT CONTROLLER. DYNAMIC, BUT WITH GOOD PROVISIONS FOR DATA RETENTION ON POWER DOWN. EXCELLENT POWER-DOWN SPECS.
1802, 1804 1805, 1806	RCA (HUGHES)	ORIGINAL 8-BIT CMOS μP. STILL GOING STRONG. NEW MODELS ARE 1-CHIP VERSIONS WITH ENHANCEMENTS.
IM 6100	INTERSIL (HARRIS)	CMOS IMPLEMENTATION OF DEC'S PDP-8 12-BIT MINI. ONLY MODERATELY SUCCESSFUL AND NO LONGER VIGOROUSLY SUPPORTED. HAS SOMEWHAT HIGH STATIC LEAKAGE. (INCIDENTALLY, DEC OFFERS CMOS VERSION OF ITS PDP-11.)
80C85	OKI (EXPECT OTHERS)	DROP-IN CMOS VERSION OF NMOS 8085. APPARENTLY NOT INTENDED FOR POWER-DOWN OR BATTERY OPERATION.
NSC800	NATIONAL (SMC)	COPIES INSTRUCTION SET OF Z80 BUT HAS BUS MODELED ON 8085. HAS HEAD START OVER OTHER MAINSTREAM 8-BIT MULTICHIP μPs AND HAS CHANCE OF BECOMING AN INDUSTRY STANDARD.
65C02 65C102 65SC0X	ROCKWELL (SYNERTEK, COMMODORE, SUPERTEX, GTE, NCR)	EXPECT SMALL CHIP AREA FOR ECONOMY AND IN SOME CASES HIGH PERFORMANCE. SOME MODELS WILL BE DROP-IN REPLACEMENTS; ALL WILL HAVE ENHANCEMENTS. ALSO 1-CHIP VERSIONS. COMMODORE CHIP DYNAMIC, WITH 0.001- TO 1.5-MHz CLOCK.
6301 (6801)	HITACHI	AMBITIOUS CMOS VERSION OF MOTOROLA 6801 1-CHIP μC. ALTHOUGH A DYNAMIC CIRCUIT, HAS MEANS TO SAVE RAM CONTENTS.
NS16C032 NS16C010 NS32C132	NATIONAL (FAIRCHILD?, SYNERTEK?)	EXAMPLE OF PLANNED USE OF CMOS ON LARGE, VERY DENSE VLSI CHIPS TO KEEP HEAT DOWN.

NOTES:
1. — = NOT APPLICABLE, NA = ACCURATE INFORMATION NOT AVAILABLE.
2. CAUTION IS ADVISED IN USING DATA IN THIS TABLE. MUCH OF THIS INFORMATION HAS NOT BEEN PUT INTO FORMAL SPECIFICATIONS AND CAN ONLY BE OBTAINED ACCURATELY FROM CHIP DESIGNERS. FURTHER, THERE IS A DANGER OF UNFAIR COMPARISONS; FOR EXAMPLE, THE QUESTION OF WHETHER CLOCK SPEED EQUALS INTERNAL BUS SPEED.

parts, each is now also available (or soon will be) in a ROMless CMOS version, so that designers can do prototyping and short-run production by using them with the growing number of CMOS EPROMs, such as the 27C16 and 27C32. (These new CMOS EPROMs, by the way, fit into the design picture very nicely: They can be used in currently available EPROM programmers because their central NMOS arrays are identical to those of their NMOS counterparts.)

The CMOS versions of the COP and 146805 families should be especially welcome to designers of small battery-operated controllers because they permit economical production of such products in small runs. By contrast, attempting to design these products with high-volume masked-ROM-only parts like the Sharp chips demands a large up-front investment.

The COP CMOS devices are strictly static and close to classical CMOS, according to a chip designer at work on this project. Some have been available in metal-gate CMOS for several years, but the plan is to phase in National's new double-polysilicon silicon-gate CMOS. Parts already out in the new double poly are spec'd several times faster than their NMOS predecessors (the 410C has a 4-μsec instruction cycle, compared with 16 μsec for the NMOS 410).

For designers who can't wait for a CMOS COP version or who don't want to pay a 30 to 50% price premium, the 498 RAT (CMOS timer and memory) part in the COP family offers a clever intermediate approach. This CMOS chip can function as a sort of coprocessor with an NMOS COP CPU, allowing the NMOS part to be periodically shut down.

The NMOS host CPU communicates with the RAT over a 3-wire serial bus, and the RAT responds to commands from the host. The host copies its own RAM data into the RAT for safekeeping and sets up the RAT's clock for powered-down mode. The RAT then takes over and switches off the host's power supply, executes the timeout and switches the host's power back on. An interrupt or override input to the RAT can

CIRCUITRY		POWER-DOWN MODES				POWER USED	
STATIC? CLOCK (MHz)	CMOS? P:N RATIO	GO TO SLEEP: HARD (PINS)	GO TO SLEEP: SOFT (INSTR)	WAKEUP: HARD (PINS)	WAKEUP: SOFT (INSTR)	CURRENT DRAIN: DYNAMIC (mA/MHz)	CURRENT DRAIN: STANDBY (μA)
YES (0–1)	YES (50:50)	NO	NO	NO	NO	1.5	0.005
YES (0–0.09)	YES (50:50)	NO	YES (CEND)	NO	NO	(10–12 μA AT 32 kHz & 1.5V)	1.5
YES (0–0.25)	YES (50:50)	YES (CKO)	YES (HALT)	YES	NO	1.0	1–10
YES (0–1)	NO (40:60)	NO	YES (STOP & WAIT)	YES (INT)	NO	4.0	1–100
NO (0.1–6)	NO NA	YES	YES (HALT)	YES (INT)	NO	1.0	1000 & 1
YES (0–6)	YES (50:50)	YES (WAIT & CLEAR)	NO	YES	NO	1.0	50
YES (0–5.7)	NA	YES (RUN, RUN/HLT & WAIT)	YES (HLT)	YES	NO	0.5	100–800
NO (0.5–3)	NO (NA)	NO	NO	NO	NO	1.0	NA
NO (0.032–5)	NO (40:60)	YES (PS)	NO	YES (PS)	NO	4.0	2000
YES (0–4)	NA	NO	NO	NO	NO	1.0–4.0	10
NO (0.1–1)	NO (NA)	YES STB	YES (SLEEP)	YES (STB & INT)	NO	6.0	1000 & 100
NO (NA)	NO (NA)	NA	NA	NA	NA	NA	NA

CMOS types fall into three basic categories

repower the host in an emergency. You can see that the RAT effectively implements the go-to-sleep and wake-up features found in CMOS CPUs, including those in the COP family.

Meanwhile, the ROMless CMOS version of Motorola's 6805 family, the MC146805E2, has several features in its favor. It's now a proven device whose price has dropped from $45 to $6.60 (100). At least one board-level supplier exists. And most reassuring, it will have a second source with an excellent reputation in CMOS—RCA.

The NMOS 6805 μC is a cut-down version of Motorola's 6800, with just one accumulator and a short 8-bit index register. At the same time, it adds some efficient bit-test instructions. These architectural and software tradeoffs have aided fabrication of the chip's CMOS version: They have kept chip size down while enhancing controller performance. The CMOS version especially shines in its well-thought-out power-down and restart modes; the early RCA 1802 and Intersil 6100 μPs, although static, did not have the controls for automatically powering down and restarting (RCA says some new 1802-family members will).

The 146805 is not only static, but also has the means to fully utilize that feature. For example, it can put itself into two different power-down modes (Wait and Stop) and be reawakened from each.

In the Stop mode, the STOP instruction actually shuts down the clock oscillator so that the chip is totally dead, affording minimum power consumption. However, because the chip is static, the on-board RAM retains its data. In this mode, the device only draws quiescent or leakage current, which can be at the microamp level (nanoamps for selected devices).

The chip can be awakened from this complete hibernation by either a reset or interrupt input. Reawakening by interrupt is the most impressive method, because then the 146805 can continue from the instruction at which it left off. When these inputs toggle the μC's clock-control flip flop, a delay occurs to assure that the clock has come up to stable oscillation before regular execution begins. The 146805's own timer counts out 1920 clock-oscillator cycles before allowing the μC to vector to the respective service routines.

In Wait mode, evoked by the WAIT instruction, the clock remains running so it can drive the on-chip timer to determine the Wait-state duration. Disconnecting the CPU from the clock stops it. Because the clock and timer remain running, power consumption is higher in this mode—but still less than 1 mW. The chip can be awakened from Wait by the timer interrupt as well as by a reset or interrupt as in Stop.

Although the 146805 is static and specs very low quiescent power, don't assume that it's pure CMOS. It

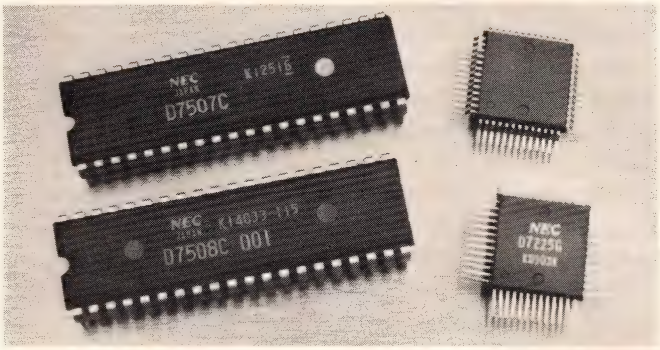


Fig 6—The use of CMOS portends a trend *to smaller package size. NEC offers flat packages (shown next to standard DIPs) for the 80C48 single-chip μC as well as for the firm's 4-bit μCs. And Motorola offers its 146805 in a leadless chip carrier. Because CMOS runs cool, designers will thus be able to squeeze their systems onto smaller pc boards and into smaller enclosures, saving money in the process.*

uses extremely-high-resistance (many hundreds of megohms) polysilicon resistors as loads for the NMOS flip flops in its on-chip RAM array. Thus, it could be vulnerable to high operating temperatures, although second source RCA says recent research might solve the poly load resistors' vulnerability problem.

Another key CMOS device is the 80C48 single-chip μC. This part holds a special significance with respect to CMOS: It was the first NMOS processor to be converted to CMOS; about 4 yrs ago, Intersil designers first attempted such a conversion. Intersil struggled vainly for several years to produce its 87C48 EPROM version with acceptable yield and finally set it aside for the simpler masked-ROM 80C48. But according to current competitors, the firm only succeeded in making users wary of whether any economically viable CMOS version of the widely used 8048 could ever be produced.

That wariness is receding. Currently, NEC says it is the leader in 80C48s, having delivered some 200,000 parts since last year. NEC's device costs 70% more than the NMOS 8048—$5.50 vs $3.00 (1000) (not counting the mask charges for either version).

The NEC 80C48 is a dynamic part with a minimum clock rate of 100 kHz. It can, however, enter a power-down mode, in which the key registers get saved and the power drain equals 10 μA typ. The device's spec'd temperature range is just −40 to +85°C, but down-hole-instrumentation customers have found that it works to 150°C with clock derating.

National, Intel and Toshiba are also in the 80C48 picture, and many other firms promise to follow suit. You can assume that because the NMOS 8048 is the most broadly second sourced of all processors, its CMOS version will likewise have the most sources.

This large number of second sources might not help users as much as they might expect, though, because each second source is taking its own approach. Thus, although all parts will be 99% identical, the hardware

and software embellishments designed to take advantage of CMOS power-down features will be different. And these power-down differences will go beyond the many internal differences in CMOS processing and circuit techniques, which themselves might or might not be transparent to users.

NEC admits its parts differ from Intel's and other firms' because they use a fairly ambitious power-down scheme whereby a 2-bit control word gets formed with the inputs from a hardware pin and a HALT instruction. This approach, it says, permits a user to choose among several power-down tradeoffs. For example, most of the chip can be left running, but the I/O can be shut down, lowering power-supply current to 2 mA from 6 mA (at 6 MHz). Alternatively, the user can choose a "deep coma" mode, shutting everything down but the data-save registers, which get put on 2.7V standby, cutting the device's drain to 10 μA.

You will in practice also note very large variations in the minimum power drains of all the CMOS 8048s, regardless of the supplier. Not only will the asleep drain increase with increasing temperature, as you'd expect, but the asleep drains for individual chips will vary widely (selected NEC parts are reported to spec 250-nA asleep drains).

How will you be able to deal with the apparent incompatibilities among CMOS 8048s? In what might be one step toward a solution, NEC says it and Intel have joined to work on a future 80C48 that will be a superset of their current versions and will have identical go-to-sleep and awake modes. Part of this standardization might include a common version of NEC's small flatpack—a very-low-profile square package, about the size of a quarter, with 11 leads on each of four sides.

Meanwhile, of the two original CMOS μPs, the RCA 1802 and the Intersil IM 6100, only the 1802 remains vigorously supported. RCA and Hughes are in the process of rounding out the single-chip additions to this family: the 1804, 1805 and 1806.

The 1802 has several compelling strengths of interest to designers with an immediate need for extreme reliability in harsh environments. It has an enviable record for successful performance in space exploration, for example. And on earth, it has survived for useful periods in the 200°C of oil-well down-hole use.

Some time will pass before any of the new CMOS μPs or μCs can match this performance. And in some cases, they might never be able to equal the 1802's harsh-environment performance because of the semi-CMOS compromises used to keep their chip size small.

The 1802's main shortcoming is the family's unusual architecture. Yet many of the designers who use the device term this architecture "brilliant," and to them it's the secret of why the 1802 is able to run high-level interpretive languages such as FORTH so efficiently. Meanwhile the device's continuing high sales volume—several million units per year—assures its continued availability.

The 1802, however, is a rather specialized device. And it seems logical that for most designers, the greatest activity will occur in the CMOS versions of more mainstream 8-bit NMOS machines. For the past several years, the Z80 and the 6500 have been the highest volume NMOS units, so you can expect the greatest amount of activity to occur in the CMOS versions of these two families.

In this regard, it looks like National could have a winner in its NSC800, a CMOS version of the Z80 with the 8085's multiplexed address/data bus. Several suppliers for the STD Bus line are putting out boards based on the 800, and they are even working on a proposed standard for CMOS use on the STD Bus that favors the 800 (**Ref 3**).

The 800 is definitely not a classical static CMOS chip like the RCA 1802; National freely admits that it has intentionally used a 40:60 p-to-n transistor ratio and that much of the chip's logic is dynamic 2-phase NMOS. The minimum clock speed is about 32 kHz (so the device can function with watch crystals). National's motiva-

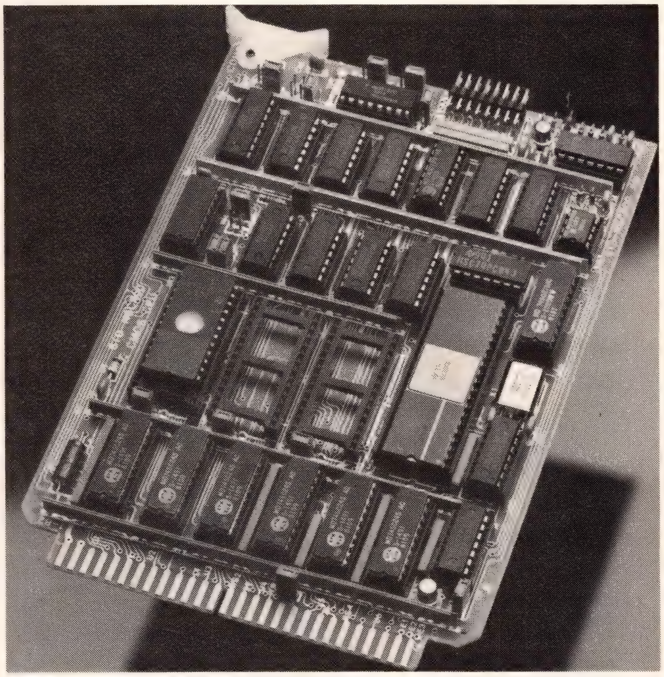


Fig 7—CMOS is finding increasing use *at the board level. This STD Bus CPU card from Baradine Products (North Vancouver, British Columbia) draws only 50 mA at 1 MHz. It uses National's NSC800 CMOS μP and houses three 28-pin byte-wide sockets for CMOS ROMs, EPROMs and RAM (a 24-pin 27C16 is in one). The glue parts are the new CMOS replacements for LSTTL from Mitel, National and others, as well as one or two parts from RCA's 4000 family. Because the STD Bus was defined for NMOS parts, the shutdown and restart controls for power saving must be implemented on the card's user edge. Note the antifloat pull-up resistors next to the bus drivers; they are important in CMOS systems, where they prevent increased power drain and erratic action.*

tion, of course, is to keep die size down despite the many registers in the Z80 architecture, allowing the 800's price to eventually be competitive with that of NMOS parts.

Yet the NSC800 does promise to provide some of the low-power and high-temperature performance characteristic of classical CMOS, according to National sources (and some of the firm's customers). For example, National says the 800 operates over the full −55 to +125°C temperature range without clock derating and that it is being evaluated for use at even higher temperatures.

Because of the large, established market for Z80-type μPs, expect Zilog and other US and Japanese suppliers to compete with National in CMOS versions of the 8080, 8085 and Z80. As with the 8048, these devices

Manufacturers of CMOS μPs and single-chip μCs

For more information on CMOS μPs and single-chip μCs, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card. Essentially, any company with an MOS process is today also likely to make CMOS devices. EDN suggests that you also contact custom-MOS and gate-array houses, because some of these are now considering offering μPs and μCs as part of their circuit libraries. Many of these specialty houses concentrate on CMOS.

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94086
(408) 732-2400
Circle No 701

American Microsystems Inc
3800 Homestead Rd
Santa Clara, CA 95051
(408) 246-0330
Circle No 702

Commodore Semiconductor Products Group
950 Rittenhouse Rd
Norristown, PA 19403
(215) 666-7950
Circle No 703

Fairchild Semiconductor
4800 Patrick Henry Dr
Santa Clara, CA 95051
(408) 988-7720
Circle No 704

Fujitsu America Inc
2985 Kifer Rd
Santa Clara, CA 95051
(408) 727-1700
Circle No 705

General Instrument Corp
Microelectronics Div
600 W John St
Hicksville, NY 11802
(516) 733-3107
Circle No 706

GTE Microcircuits
2000 W 14th St
Tempe, AZ 85281
(602) 968-4431
Circle No 707

Harris Semiconductor
Box 883
Melbourne, FL 32901
(305) 724-7000
Circle No 708

Hitachi America Ltd
1800 Bering Dr
San Jose, CA 95131
(408) 292-6404
Circle No 709

Hughes Aircraft Co
Solid State Products Div
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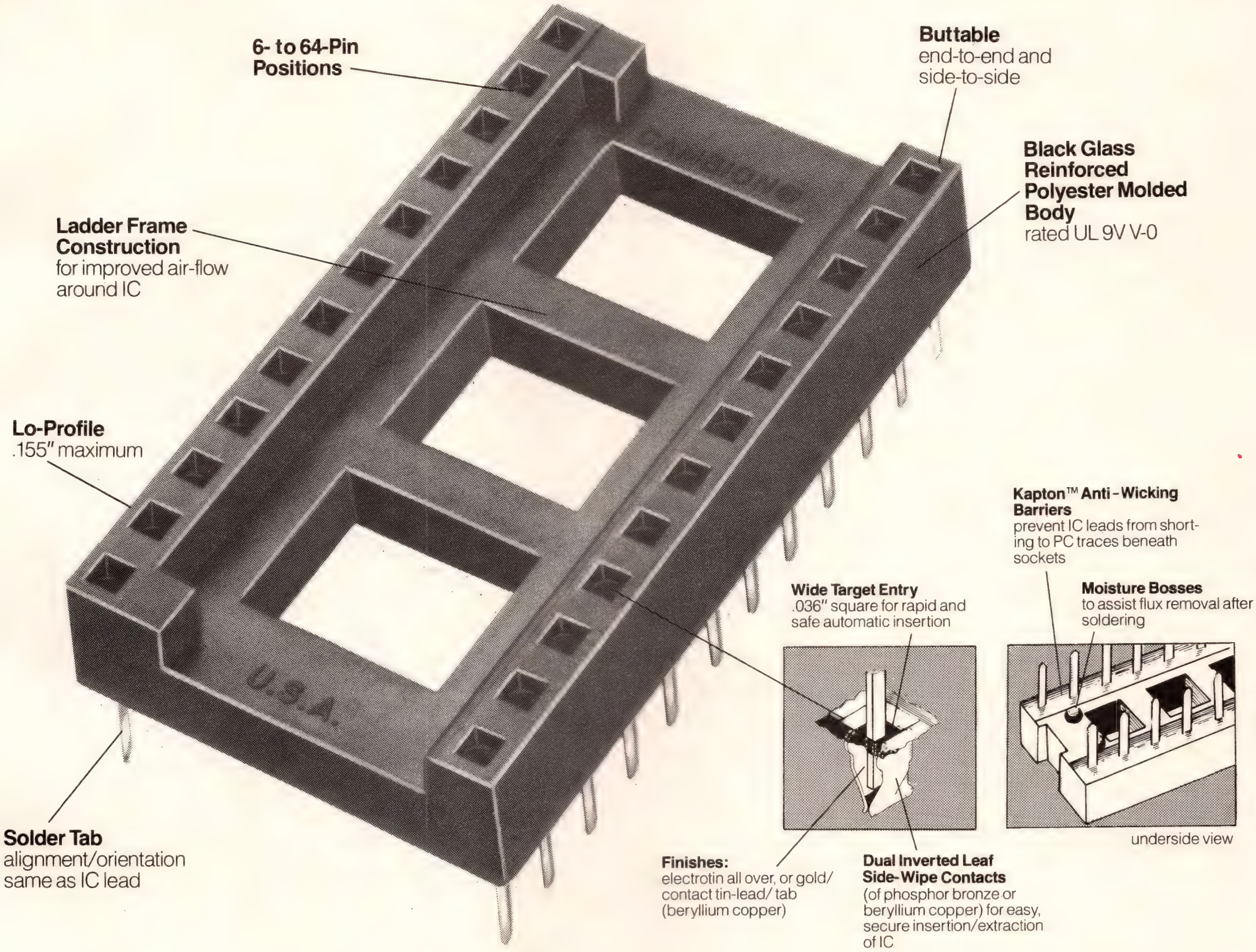

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CIRCLE NO 38

will be only 99% alike—and that 1% difference could drive users crazy.

Turning to the 6502, note that its architectural features are well suited to efficient conversion from NMOS to CMOS. The device has a small chip area in NMOS, and it's fast. The small NMOS chip size makes for a small, producible CMOS chip, and the NMOS part's throughput will be enhanced in the CMOS versions because their finer geometry will allow them to run at faster clock rates.

At least four CMOS versions of the basic multichip 6502 μP will be available, along with some CMOS versions of Rockwell's 6500/1 single-chip-μC variant. Three of these will come from the current sources of the NMOS 6502: Commodore/MOS Technology, Rockwell and Synertek. In addition, Supertex, a company that has never produced an NMOS 6502, plans a CMOS version. The devices are in varying stages of completion and should be introduced late this year or sometime next.

A survey of the suppliers reveals that, as with the 8048 and NSC800, differences will exist among these CMOS versions. For example, Rockwell, Supertex and possibly Synertek plan static devices, but Commodore has elected to use dynamic circuitry and so will have a minimum clock speed.

Rockwell is particularly bullish about its CMOS 6502. This chip might actually turn out to be smaller than its NMOS predecessor, thanks to its finer geometry (3 μm, compared with 5 μm in the original). Rockwell also expects a very low dynamic dissipation—the spec will start out at 4 mA/MHz but could test out at 1 mA/MHz.

Rockwell and Supertex are promising 4-MHz speed for their CPUs. This speed, along with the 6502 architecture, could force the use of expensive fast-access memories (85-nsec access time). Therefore, Rockwell says it will produce a special part, the 65C102, that will bring out the ϕ_4 system clock rather than ϕ_2 as on the 6502. This feature will stretch access time to 170 nsec.

Commodore is taking a different tack, aiming its CMOS 6502 at the handheld-computer market, which requires only moderate clock speeds to keep operating power consumption down but also requires a highly producible, economical chip. As a result, Commodore's chip designers say they have remained with their 6-μm process and only expect to achieve a 1.5-MHz clock speed.

A factor to watch in all forthcoming CMOS versions of μPs and single-chip μCs is the degree to which they might be able to change their instruction sets to deal with competition. Already, keen competition is occurring among suppliers as they try to outdo each other by providing software features. Chip designers say that everyone is using microcoded instruction-decode ROMs (invariably in dynamic NMOS arrays), so it should prove much easier for suppliers to juggle their additional instructions. Therefore, expect a great deal of competitive jockeying over the next few years with respect to the additional instructions used in the CMOS machines. Nobody yet knows which of these CMOS embellishments to the NMOS devices will become standard features. EDN

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3. Anderson, Garry J, "Proposed CMOS STD Bus Specification" (March 29, 1982 revision), Baradine Products Ltd, Box 86757, North Vancouver, British Columbia, Canada V7L 4L3. (See also "CMOS STD Bus Proposal," May 25, 1982, from the same source. These documents are worth having even if you are not interested in the STD Bus, because they shed light on problems encountered in switching from NMOS μPs and TTL glue parts to CMOS μPs and CMOS glue parts.)
4. Huston, Bill, "Practical CMOS Microprocessor Systems," *AFIPS (NCC) Conference Proceedings,* June 7-10, 1982, Houston, TX. (Excellent detail on designing the 146805 μC into systems by an advocate of that CMOS device. Obtain from the author at Motorola (Austin, TX) or from AFIPS Press, 1815 N Lynn St, Arlington, VA 22209.)
5. "C-44 Bus Newsletter," Spring and Summer 1982. Obtain from Synapse Corp, Box 1016, North Falmouth, MA 02556. (Readable, informative 4-pg pamphlets on the use of the 146805 and NSC800 in battery-operated micropower instrumentation.)

Acknowledgements

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	HM-65161-2/8	−55 to +125°C	200 μA	500 μA	70 ns
Synchronous	HM-6516B-9	−40 to +85°C	25 μA	50 μA	120 ns
	HM-6516B-2/8	−55 to +125°C	50 μA	100 μA	120 ns
	HM-6516-9	−40 to +85°C	50 μA	100 μA	200 ns
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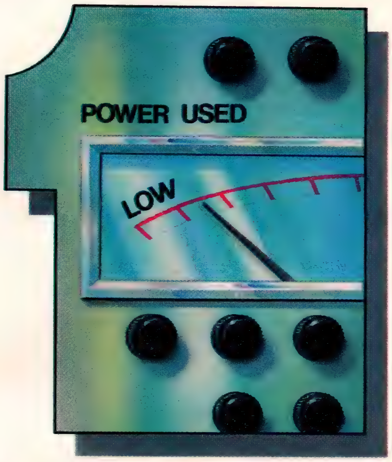

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* Guaranteed over full industrial and military temperature and voltage ranges. † Winter, 1982 ‡ Spring, 1983

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CIRCLE NO 39

Analog design techniques suit process-control needs

Although analog circuits are relatively inflexible, they can furnish process-control systems with operational features comparable to those attainable using digital methods. A stepper-motor pump-drive application illustrates the techniques involved.

Jim Williams, National Semiconductor Corp

For many process-control applications, analog control circuits prove a better choice than their digital counterparts, especially when you expect low product volumes and when fast design time and high noise immunity are design priorities. In fact, if you're working with well-defined operational specifications and don't anticipate having to make major modifications, analog methods serve as viable alternatives to intelligent but dedicated and expensive hardware/software approaches.

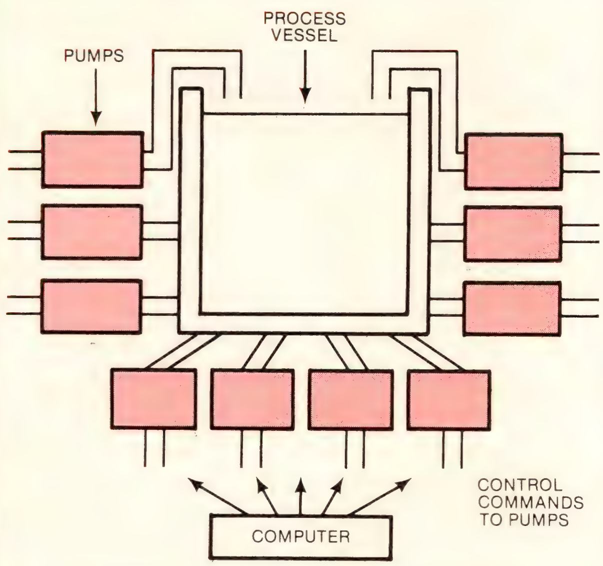


Fig 1—In this conceptual computer-controlled chemical-mixing system, *the computer governs several pumps delivering chemicals to the process mixing vessel by periodically sending updated pulse-width-modulated commands that control the pumps' speeds.*

Controlling a pump's speed

To demonstrate, this article describes the design of an analog pump controller that manipulates computer-generated command pulses to regulate stepper-motor-driven pumps in a critical chemical-mixing process. The controller/pump system furnishes precise fluid delivery at both fast and slow rates, a requirement often arising in chemical and biological process-control systems, which demand high pumping rates for flushing or process startup and slow but accurate flow rates for mixing precise amounts of liquid. Although dc motors can deliver adequate high-speed performance, they often need complex and expensive digital control to perform well at very slow speeds. In contrast, exponentially driven stepper motors can easily handle a pump's conflicting high- and low-speed drive requirements.

Fig 1 diagrams a computer-driven system that governs several pumps feeding an intricate chemical process. The computer controls each pump's speed by periodically sending a pulse-width-modulated control command. Because the computer runs in a time-shared manner, each pump controller must retain the last received pulse width's value.

In this application, each pump gets speed-updated every 30 sec by a 50- to 1000-msec pulse. The pump drive must provide optimum speed-setting resolution for the low-speed ranges to provide increasingly slower

flow rates as the system approaches crucial mixing conditions. And the controller must possess a high degree of noise immunity to prevent spurious noise-induced responses from degrading process quality.

Fig 2 illustrates a μP-based-controller scheme. In this arrangement, the computer delivers an input pulse that gates a clock. The clock in turn serially loads a bank of parallel counters that determine the input pulse width. The counters address a processor section that converts input data to a frequency output, using an exponential transfer function—a nonlinear response that achieves the required high resolution (precise liquid delivery) at slow pump speeds. Finally, the frequency output activates a stepping-motor driver that runs the pump.

On the surface, this digital controller's operation appears relatively simple. However, the application masks some tricky design problems. For example, the lengthy period between speed updates, coupled with the need to avoid erroneous pump responses, mandates careful power-supply design, including provision of such functions as RFI filtering, memory battery backup and self-checking software.

In addition, the need for a high-resolution, smoothly varying frequency-output function demands careful design attention to how the processor synthesizes its

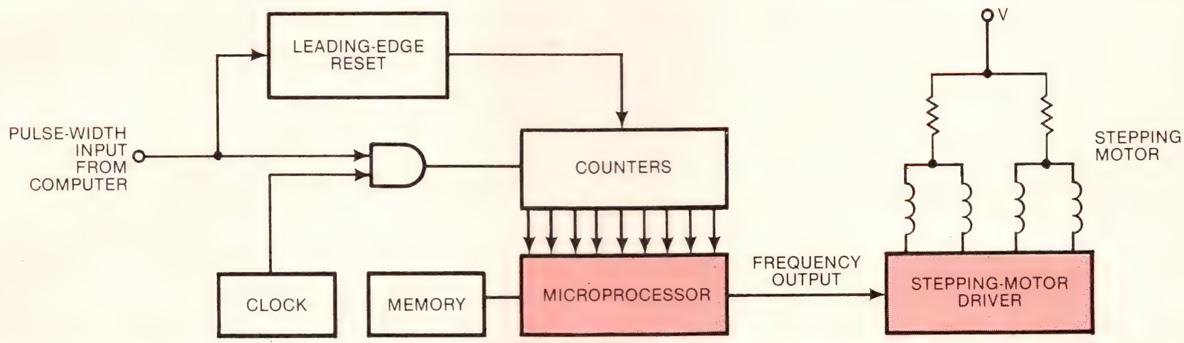


Fig 2—Upon receiving gated pulses, *a μP converts timed computer data into a frequency output, using an exponential transfer function. This nonlinear response results in the necessary high-resolution-at-low-speed characteristics for accurately controlling pump operation with a stepper-motor driver. The problems that can arise with this digital approach to controlling* ***Fig 1****'s mixing system include noise sensitivity, memory-retention difficulties and an undesirable quantized frequency-shift characteristic.*

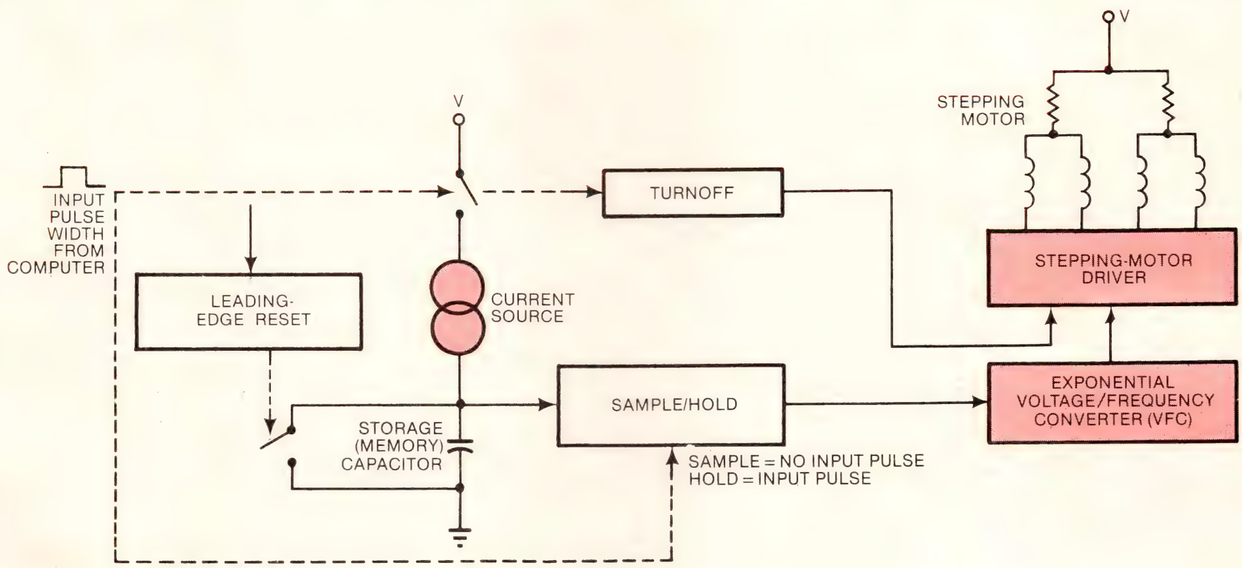


Fig 3—In this analog-pump-controller approach, *a computer's command pulses direct a current source, which in turn charges a storage capacitor that provides noise-immune analog-data retention. When the command pulse ceases, the sample/hold amp receives the capacitor's stored voltage and delivers it to the exponential voltage-to-frequency converter (VFC). The VFC activates the stepper-motor driver in a continuous, smooth manner; the turn-off stage deactivates the motor driver.*

output. Although these problems are amenable to solution, they complicate the controller's design and entail lengthy development time and high cost.

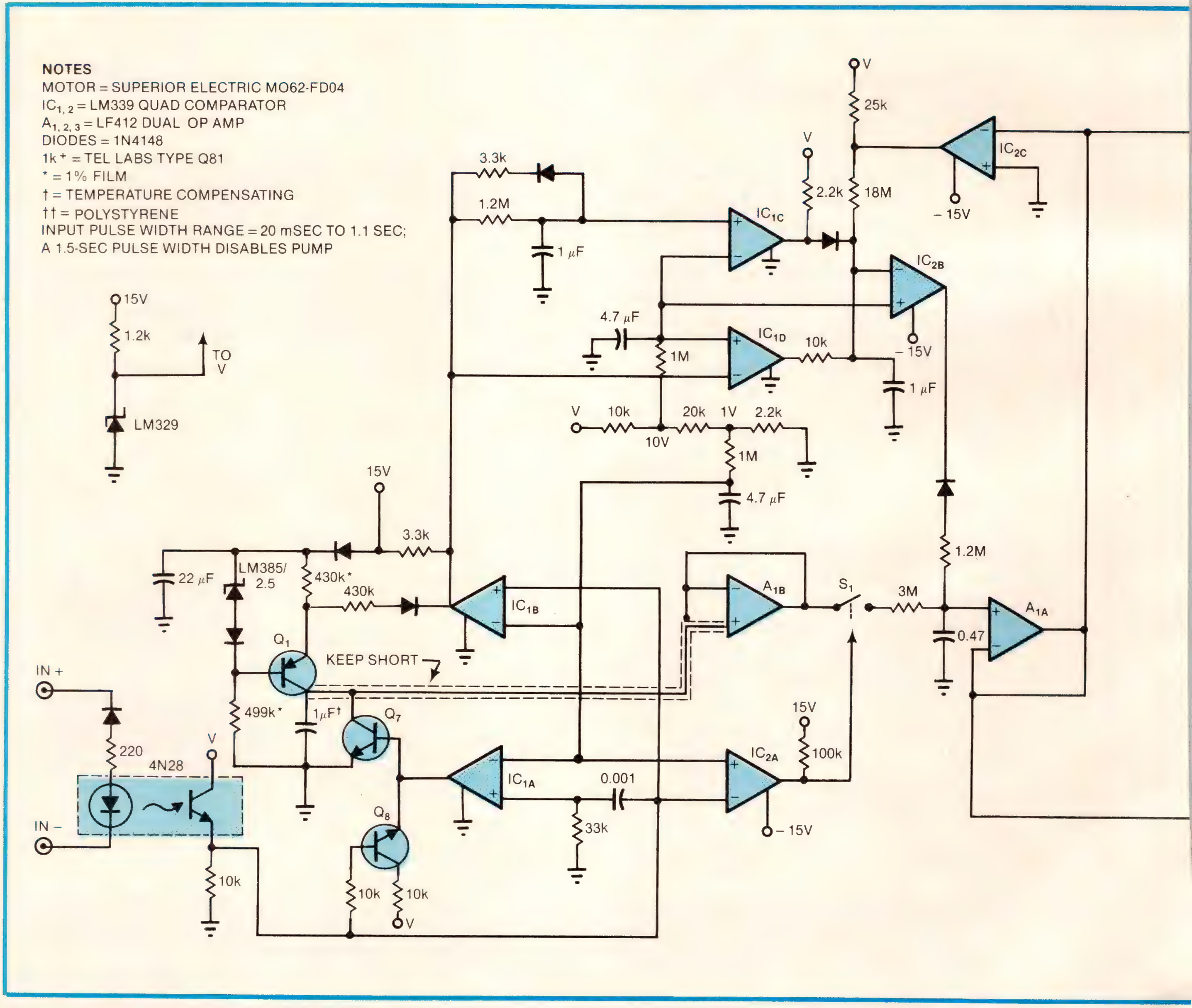
Take the analog route

Considering the task's conceptual simplicity, however, reveals a clear edge for an analog-control approach to satisfying this application's critical requirements. A turnkey system, it needs little intelligence or flexibility and can employ a straightforward data-retention structure. And although the digital μP-based approach can also meet these requirements, it involves substantial hardware and software overhead to overcome noise-immunity and frequency-shift-resolution problems.

The analog-based design surmounts these obstacles, providing inherent noise immunity and superior frequency-vernier capability. More important, though, an analog approach eliminates the intensive software effort required by μP-based methods. As a matter of record, the analog pump-controller design was conceived, breadboarded and released for production in just 4 wks—and at a cost competitive with an alternative μP-based method.

Fig 3 depicts the analog system. In this scheme, a capacitor furnishes memory storage. An exponentially responding voltage-to-frequency converter (VFC) fulfills the function of **Fig 2**'s processor. In operation, the computer's command pulse gates a current source that linearly charges the storage capacitor. While the capacitor is charging, the sample/hold stage enters Hold mode, blocking the capacitor's ramping action from the VFC.

When the command pulse just ceases, the capacitor achieves a voltage level that the sample/hold accepts



and feeds to the VFC. By issuing an extremely wide pulse, the computer actuates the turn-off stage, which deactivates the stepper-motor drive.

Optoisolation eliminates noise

Fig 4 shows the analog pump controller's schematic diagram. To initiate circuit action, the computer sends an input pulse to the 4N28 optoisolator, which eliminates noise-pickup-induced ground-loop and data-line problems. Appearing at its emitter, the optoisolator's output (**Fig 5,** waveform A) goes to IC_{1A} and IC_{1B}. IC_{1A}'s differentiator setup—a 0.001-μF/33-kΩ combination—generates a short pulse (**Fig 5,** waveform B) that biases Q_7. This transistor in turn resets its associated 1-μF capacitor (**Fig 5,** waveform C).

Note that Q_8's emitter supplies the current to base-bias Q_7 ON because IC_{1A} is an open-collector device. In turn, Q_8 receives its base bias from the optoisolator, which provides a drive output only when a command pulse appears at the controller circuit's input. Consequently, in the highly unlikely event that a severe noise disturbance causes IC_{1A}'s output to rise, Q_7 still doesn't receive a drive pulse, and its 1-μF capacitor does not get reset.

The 1-MΩ/4.7-μF filter, which feeds IC_{1A}'s minus input, provides additional noise immunity by ensuring a stable trip point during noise disturbances. The optoisolator's output also goes to IC_{1B}, which gates the Q_1 current source. When Q_7 turns off, its 1-μF capacitor immediately starts to ramp up (**Fig 5,** waveform C). (Circuit-operation speed in **Fig 5** has been increased to provide optimum waveform photographs.) Then, the A_{1B} follower unloads the capacitor.

Diode/capacitor decoupling of Q_1 assures high noise

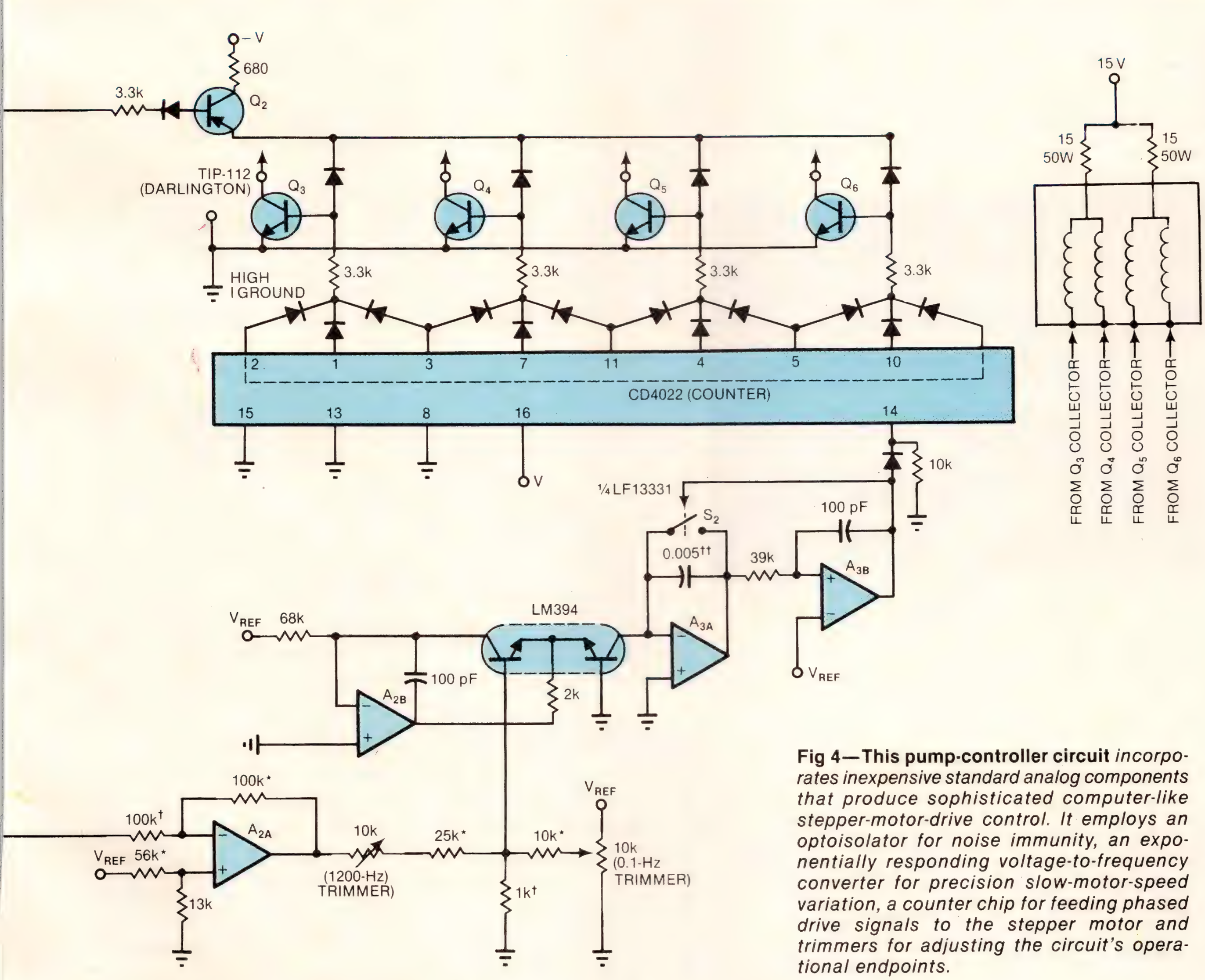


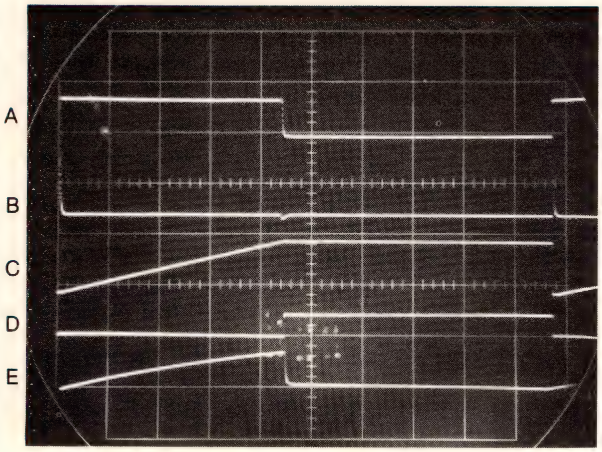
Fig 4—This pump-controller circuit *incorporates inexpensive standard analog components that produce sophisticated computer-like stepper-motor-drive control. It employs an optoisolator for noise immunity, an exponentially responding voltage-to-frequency converter for precision slow-motor-speed variation, a counter chip for feeding phased drive signals to the stepper motor and trimmers for adjusting the circuit's operational endpoints.*

rejection, even for supply dropouts, during the capacitor's ramp time. During ramping, IC_{2A}'s output stays LOW and shuts off S_1. This switch maintains A_{1A}'s output at a dc level. When the controller's input pulse ceases, IC_{1B}'s output goes LOW and disables Q_1. The integrating 1-μF capacitor therefore stops charging. Concurrently, IC_{2A}'s output goes HIGH and closes S_1. As a result, A_{1A}'s output changes to the capacitor's newly acquired level. Located in A_{1A}'s input section, the 3-MΩ/0.47-μF filter provides a time constant that limits the stepper motor's acceleration rate, thereby preventing stalling.

Try an exponentiator

Op amp A_{1A}'s output feeds the A_2-A_3 configuration, which forms an exponentially responding VFC that controls the input current to the A_{3A}-A_{3B} integrator-comparator-type oscillator stage. To accomplish this function, A_{2B} and the LM394's dual transistors constitute a voltage-input, current-output exponentiator in accordance with transistor V_{BE}-vs-I_C characteristics.

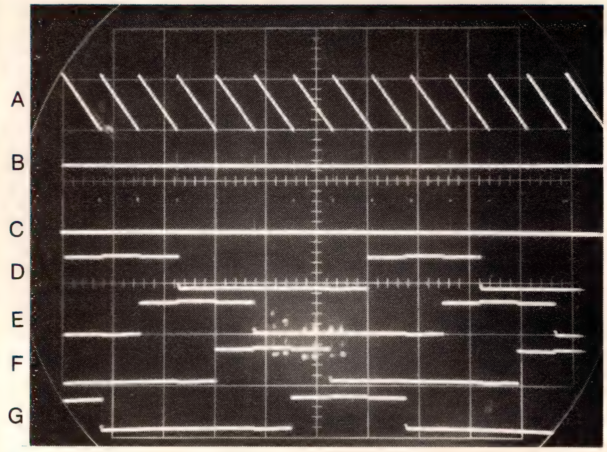
The 1-kΩ temperature-compensating resistor connected to the LM394 thermally compensates for the



TRACE	V/DIV
A	20
B	10
C	5
D	50
E	10

HORIZONTAL SWEEP-
1 mSEC/DIV

Fig 5—Important waveforms *found in the analog pump controller's input section include the 4N28 optoisolator's pulsed emitter output **(A)**, IC_{1A}'s plus input or memory-reset spike for biasing Q_7 **(B)**, Q_7's output or current-source-driven ramp for resetting the 1-μF memory capacitor **(C)**, IC_{1D}'s output pulse for shutting down the stepper-motor driver via IC_{2B} and IC_{2C} **(D)** and IC_{1C}'s plus input, which never charges above 10V for the normal range of incoming pulse widths **(E)**.*



TRACE	V/DIV
A	5
B	50
C	20
D	20
E	20
F	20
G	20

HORIZONTAL SWEEP-
1 mSEC/DIV

Fig 6—The CD4022 counter chip *in **Fig 4**'s pump-controller circuit sends properly phased frequency-modulated drive signals to the pump motor. Waveform **A**, for example, represents A_{3A}'s ramp output; waveform **B** shows A_{3B}'s positive input reset signal; waveform **C** details A_{3B}'s output pulse; and waveforms **D** through **G** depict the four phase-drive signals to Q_3 through Q_6 via diode-ANDed outputs.*

KT/Q drift factor. Similarly, the LM394's dual transistors suppress V_{BE}'s contribution to temperature error. A_{2A} biases the exponential converter's input range by combining A_{1A}'s output with the necessary offset term for proper exponentiator operation. Trimmers allow you to adjust the 1200- and 0.2-Hz endpoints.

A_{3B}'s pulse-train output contains frequency components that relate exponentially to the controller circuit's most recently received input-pulse width. It drives the CD4022 counter chip, which generates four properly phased signals (**Fig 6**) for driving the stepper.

Driving the pump

The additional sections of IC_1 and IC_2 allow the computer's command pulse to shut down the pump. For the normal range of input widths, the 1-μF capacitor at IC_{1C}'s plus input (**Fig 5**, waveform E) never charges above 10V. Under these conditions, IC_{1C}'s output always stays LOW. The only source available to charge the 1-μF capacitor tied to IC_{2B}'s minus input thus comes through the 18-MΩ resistor.

However, during normal operation, A_{1A}'s output remains positive, ensuring that IC_{2B}'s negative input

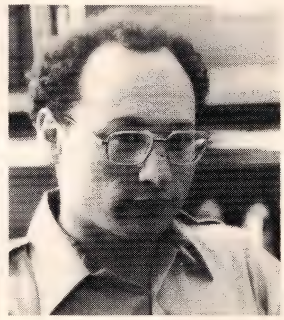
Use an optoisolator to eliminate noise effects

stays that way. This condition forces IC_{2B}'s open-collector output to float. If the controller circuit receives an input pulse substantially wider than the normal maximum, therefore, IC_{1C}'s input charges above 10V. This action quickly dumps a large charge into IC_{2B}'s 1-μF capacitor, forcing its voltage level to rise to the negative rail. This value pulls A_{1A}'s input negative, turns on Q_2 and cuts off all drive signals to the output transistors (Q_3 to Q_6).

A_{1A}'s negative output also feeds back to IC_{2C}, driving that device's output positive. This output supplies a continuous topping-off current to IC_{2B}'s input capacitor. The connection completes a positive feedback latch, which prevents the pump from operating until the counter receives a pulse width within the controller circuit's normal range. IC_{1D} functions to clear out the IC_{2B} capacitor's charging action (**Fig 5,** waveform D) as each new command pulse arrives.

The time constant associated with A_{1A}'s input section lets the controller circuit examine each received pulse and never disables this clamping performance unless the pulse width resides within established limits. Although the latch's positive feedback doesn't require the computer to send successive shutdown instructions to the pump, the controller circuit ensures that the pump's motor can't be energized, even briefly, if successive turn-off-length pulses appear. **EDN**

Author's biography



Jim Williams, now a consultant, was applications manager with National Semiconductor's Linear Applications Group (Santa Clara, CA) when he wrote this article. Before working at National, he was employed by Arthur D Little Inc and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

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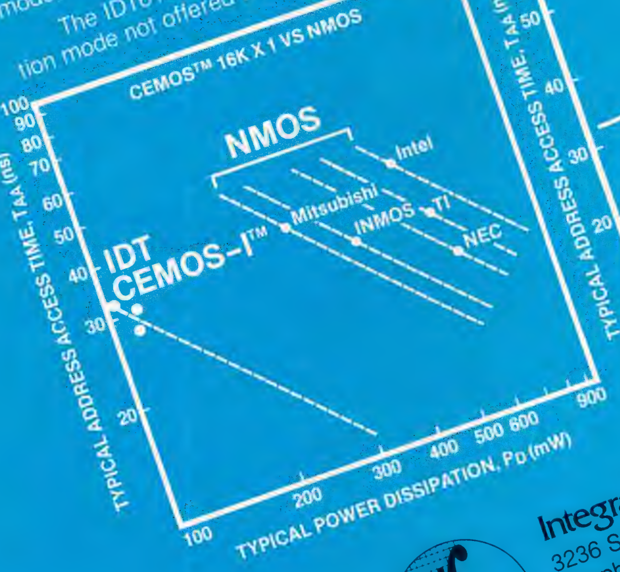

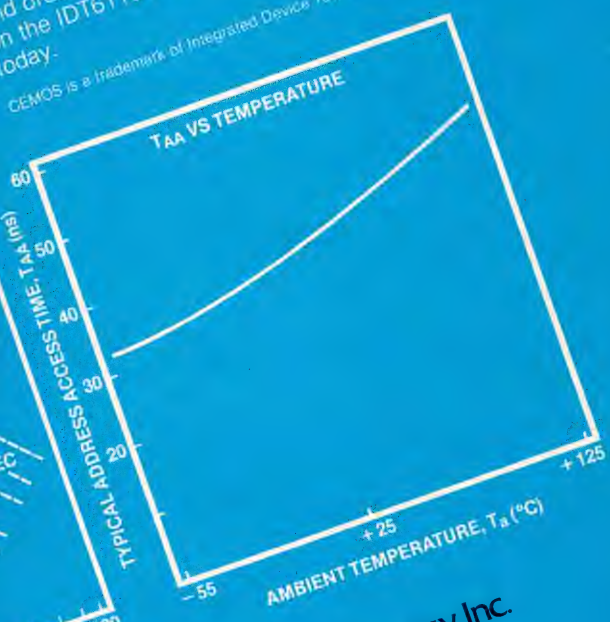

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Evaluate sensor tradeoffs in digital-thermometer design

A CMOS integrating A/D converter provides features that prove advantageous for digital-thermometer applications. But to produce the most effective design, you must also consider various sensor configurations.

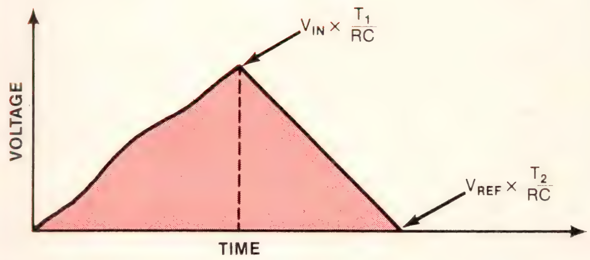
Wes Freeman, Teledyne Semiconductor

Digital-thermometer design requires consideration of signal-conditioning and display-driving circuitry as well as of temperature sensors. Using a single-chip integrating CMOS A/D converter greatly simplifies the circuitry, freeing you to concentrate on sensor selection and calibration. In choosing the sensor, you must in turn consider component cost, ease of calibration and power consumption. And because no sensor configuration is superior in all three areas, you must base your choice on labor cost, automated-test-equipment requirements and performance specifications.

Ratiometric conversion suits sensor circuits

Before choosing the sensor, though, consider the ADC's characteristics. Among the available devices, CMOS integrating A/D converters, such as the multiple-sourced TSC7126, particularly suit thermometer applications for six primary reasons:

- The integrating feature averages out noise, yielding repeatable results.
- Because of the device's dual-slope-integration and autozero features, accuracy depends only on reference absolute value and clock-pulse equality within a given conversion cycle; thus, few precision components are required.
- The converter achieves very good rejection of frequencies corresponding to integral multiples of the measurement period, thus permitting reduction of line-frequency-noise effects.
- The A/D conversion is ratiometric, and the input and reference are fully differential—a combination that simplifies interfacing to sensors.
- The converters are multiple sourced and inexpensive and require few support components. The TSC7126, for example, requires only 10 discrete components plus the display to form a complete A/D converter with a 3½-digit readout.



NOTE:
T_1 = SIGNAL INTEGRATE TIME
T_2 = REFERENCE INTEGRATE (DEINTEGRATE) TIME

$$V_{IN} \times \frac{T_1}{RC} = V_{REF} \times \frac{T_2}{RC}$$

$$\therefore \frac{V_{IN}}{V_{REF}} = \frac{T_2}{T_1}$$

Fig 1—A dual-slope integrating converter *furnishes an output that's independent of integrator time constant and clock frequency; its accuracy depends only on a reference and the equality of clock cycles within a conversion period.*

- CMOS processing reduces the power requirements to only 100 μA from a 9V battery.

Now consider the details of the dual-slope-converter circuitry. Its operation depends on an oscillator, built into the chip, that provides a basic clock timing signal. To start the conversion process, the device's integrator resets to 0V and then integrates its input for 1000 clock cycles during the signal-integrate phase **(Fig 1).** Then—during the deintegrate or reference-integrate phase—it integrates the device's reference voltage (of opposite polarity) until the integrator output voltage again reaches 0V. During this portion of the converter cycle, device circuitry counts clock pulses, yielding a counter value at the conclusion of the deintegrate phase that's independent of the integrator time constant, the

Use a low-cost diode as a temperature sensor

clock frequency and any of the other physical constants of the system; the count is proportional only to the ratio of the input to the reference, reading 1000 when the two are equal. This counter reading then drives the display.

Fig 2 shows a pinout diagram for the converter; the external components consist of an input filter (R_1 and C_1), oscillator components (R_2 and C_2), a capacitor to store the reference voltage (C_3), an autozero capacitor (C_4) and integrator components (R_3, R_4 and C_5).

Choose a sensor that matches your requirement

Usually a more complex task than converter-circuit design, sensor selection involves considering the tradeoff between cost and ease of calibration. All sensor circuits require two adjustments: one for full-scale calibration (slope) and one for calibration to an intermediate temperature. Sensors differ, however, in that some allow you to make both adjustments at room temperature while others require calibration at two temperatures. (Theoretically, a laser-trimmed sensor such as the AD590 can be used without external calibration, but low-cost thermometers typically still employ 2-trimmer configurations because the precision components required for untrimmed operation are prohibitively expensive.)

You can use an ordinary silicon diode as a sensor. It furnishes the lowest cost and power consumption (typically 125 μA at 9V), although it must be calibrated at two temperatures because dV/dT, its change in forward voltage (V_F) with temperature, is not closely controlled. The dV/dT rating of a typical diode is about −2.1 mV/°C.

Fig 3's circuit illustrates one method of using this change in V_F to sense temperature. Because the sign of the voltage change is negative, the diode voltage is applied to the TSC7126's IN LO input to produce correct polarity. R_1 offsets the diode voltage so that the display reads 00.0 at 0°C, and R_2 adjusts the reference to match the diode dV/dT.

Ideally, a current source should drive the sensor diode, but substituting a high-value resistor for a constant-current source adds only 0.75°C of nonlinearity. The resistor also provides a slight compensation for errors arising from decreasing battery voltage and reference drift with temperature.

To calibrate **Fig 3**'s circuit, immerse the diode sensor in a stirred ice/water bath (0°C) and adjust R_1 for a 00.0 reading. Then immerse the diode in boiling water (100°C) and adjust R_2 for a 100.0 reading. The requirement for making two calibrations at specified temperatures offsets the low parts cost of the diode sensor. Furthermore, because V_F versus current is seldom specified for general-purpose diodes, R_1 and R_2 must have a fairly wide adjustment range. Therefore, they should be multiturn pots.

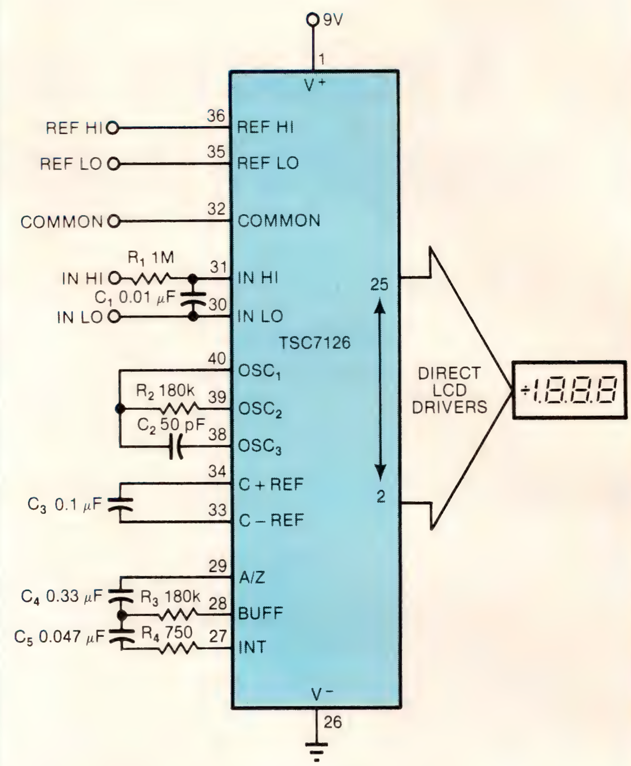


Fig 2—CMOS integrating A/D converters *such as the TSC7126 require the addition of only a few discrete components to form a circuit complete with a 3½-digit LCD.*

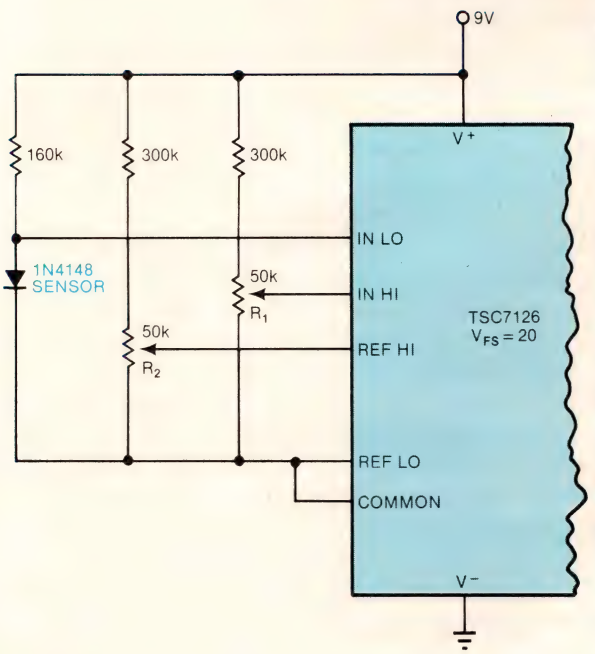


Fig 3—You can use a diode as a temperature sensor *if you want economy and low power consumption.*

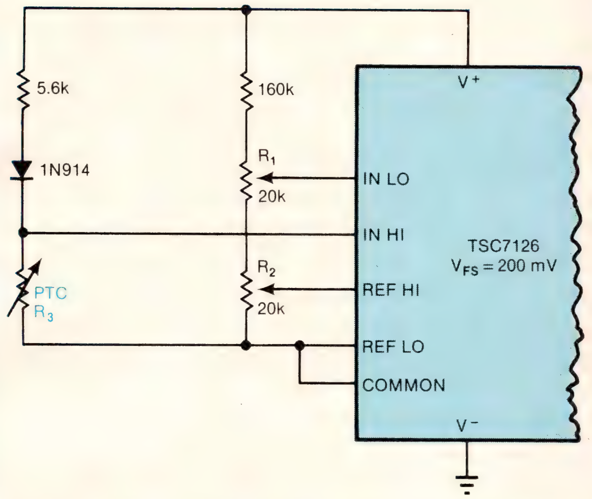


Fig 4—A positive-temperature-coefficient (PTC) resistor *makes a good sensor if you linearize it with a series diode placed in close thermal proximity to it.*

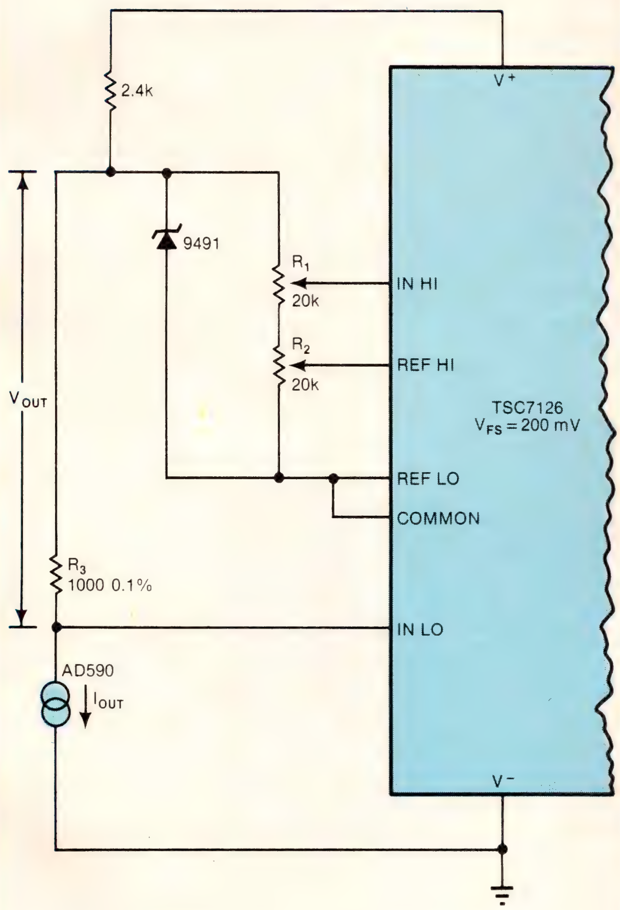


Fig 5—To simplify a digital thermometer's calibration procedure, *employ an AD590 bandgap transducer as the sensing element.*

You can simplify sensor calibration by substituting Motorola MTS Series sensors for ordinary silicon diodes. These devices are transistors with a carefully controlled V_{BE} match within device lots; they thus achieve a predictable temperature-coefficient-versus-V_{BE} characteristic. Indeed, the best grade of MTS devices exhibits temperature-matching accuracy of ±2°C over −40 to +150°C.

An MTS transistor with collector-base shorted can simply replace **Fig 3**'s diode. You can calibrate this circuit at any known temperature, although you must make some calculations. First, measure the transistor's V_{BE} and calculate its current to determine—by comparison with device data-sheet values—the deviation from the −2.265-mV/°C ideal temperature coefficient. Then, derive the required V_{REF} and adjust R_2 accordingly. Finally, set R_1 so that the thermometer indicates actual room temperature.

Use of the MTS sensor simplifies circuit calibration, but the higher cost of the MTS device offsets this savings. The level of computation required for calibration is quite low, so a programmable-calculator/DVM combination is adequate for the task.

Use a resistor's temperature coefficient

Another promising sensor candidate is the positive-temperature-coefficient (PTC) resistor. Available from such firms as Texas Instruments, these bulk-silicon devices are about the same size as a diode. They typically furnish sensitivity of 0.7%/°C.

Fig 4 illustrates a temperature-display circuit using a PTC device. Ideally, it should be biased with a current source and not another resistor, which can introduce an error of several degrees Celsius. However, biasing the PTC resistor to operate at about +2.1 mV/°C allows a common silicon diode (D_1), placed in close thermal proximity to the PTC device (R_3), to offset R_3's voltage drop and linearize the bridge.

The penalty for this linearization technique is that 300 μA of PTC-resistor current is required to produce a 2.1-mV/°C output, yielding total battery current of about 460 μA. Using a higher value PTC resistor reduces power consumption.

Calibration of the circuit is straightforward. After you determine the temperature coefficient for a given lot of PTC sensors, calculate the required reference voltage and then adjust R_2 until the voltage between REF HI and REF LO equals the calculated voltage. Finally, adjust R_1 to display ambient temperature.

Laser trimming improves performance

Sensors that employ a bandgap technique have simpler calibration schemes than do diode- and resistor-based circuits. One such transducer, Analog Devices's 2-terminal monolithic AD590, uses the highly predict-

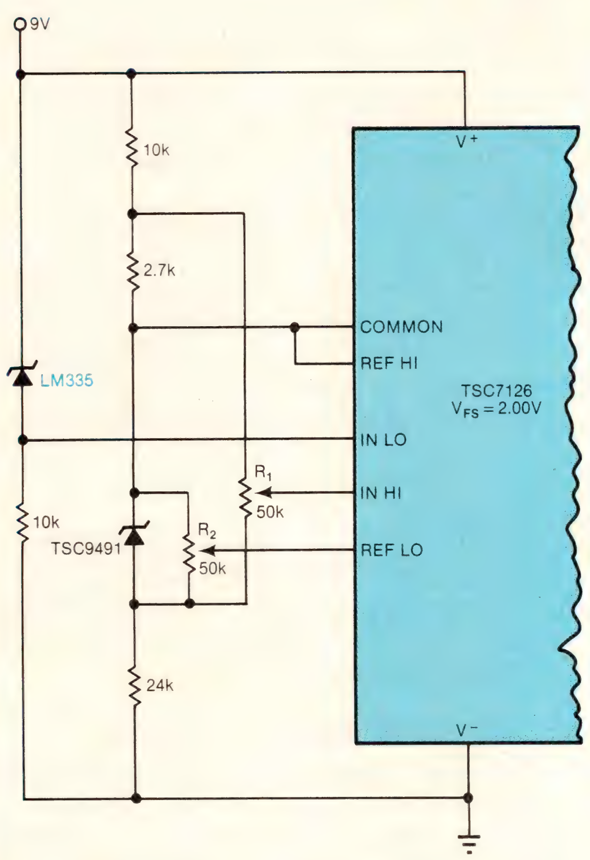


Fig 6—Eliminating Fig 5's requirement for a precision resistor, *the LM335 bandgap temperature transducer provides a voltage output rather than a current output.*

able difference in V_{BE} between two identical transistors operating at different current levels to sense temperature. The AD590 furnishes a current-output laser trimmed to exactly 1 μA/°K. Linearity of the bandgap design is excellent; even the lowest grade AD590 provides ±1.7°C linearity over −55 to +150°C.

Fig 5's circuit interfaces the AD590 to the TSC7126. Resistor R_3 converts the AD590's output current to a voltage, so it must be a precise, low-temperature-coefficient component. The TSC9491 1.22V reference biases the AD590 within the A/D-converter common-mode range, provides a very stable reference and permits offsetting of IN LO to provide a 00.0 reading at 0°C.

AD590 calibration can be performed at room temperature. First, you adjust R_2 until REF HI is 100 mV above REF LO. Then, adjust R_1 until the display reads room temperature. The simplicity of this calibration procedure is offset by the cost of precision component R_3 and the AD590 itself.

You can improve AD590-circuit performance by using a more complicated calibration procedure. First, measure the R_3 value with power off. Then, with power applied, measure V_{OUT} and calculate the actual AD590 I_{OUT}. The difference between the temperature proportional to actual I_{OUT} and room temperature in degrees Kelvin is the scale-factor (or slope) error, which, multiplied by 100°C and the actual value of R_3, yields the voltage error. Add this error voltage to the 100-mV ideal reference voltage and adjust R_2 to produce the corrected reference voltage. Finally, adjust R_1 so that the display reads the room temperature.

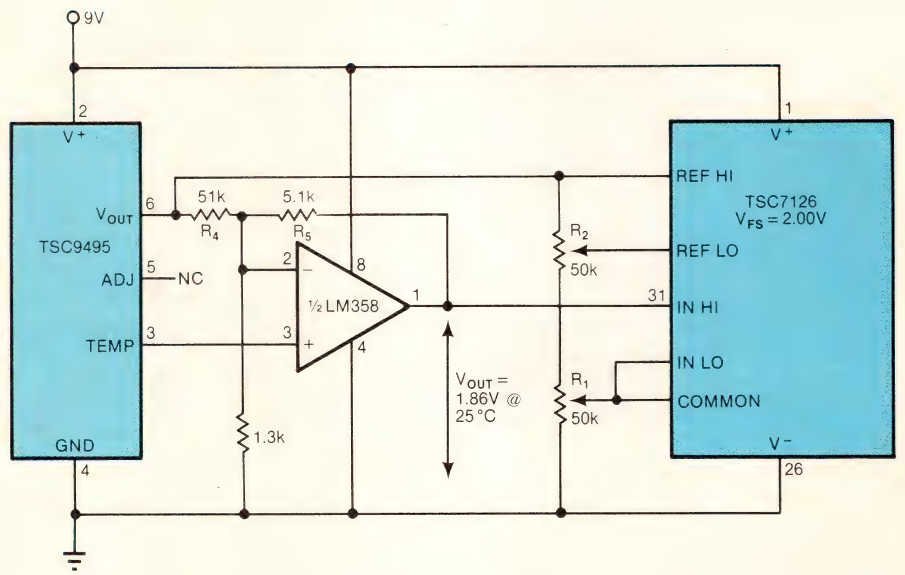


Fig 7—Suiting use in expanded-scale thermometers, *the TSC9495 furnishes a reference and output proportional to temperature.*

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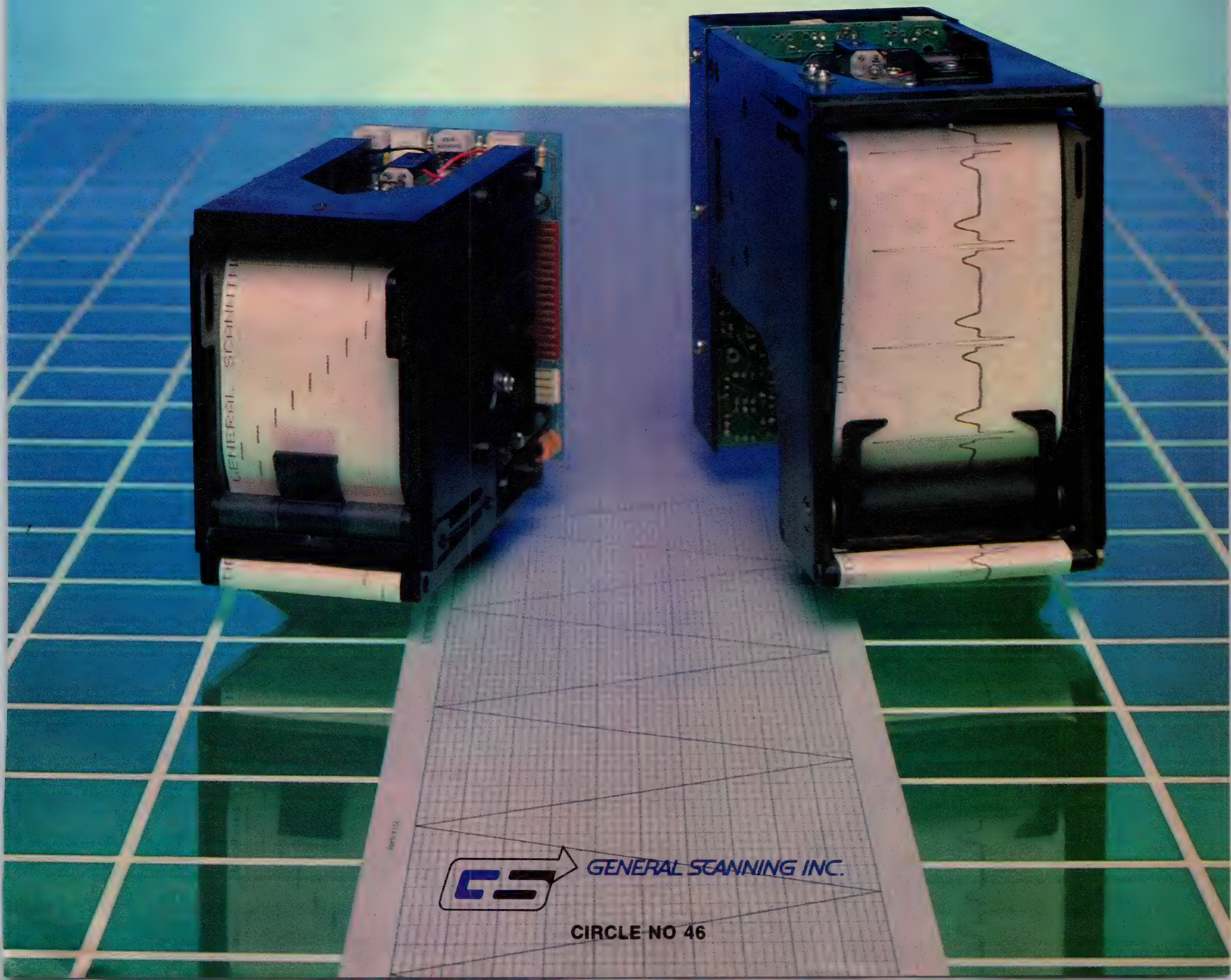

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Laser-trimmed bandgap transducers up calibration ease

The National Semiconductor LM335 (**Fig 6**) also uses the bandgap principle to provide a linear output proportional to temperature; it furnishes a 10-mV/°K voltage output, which produces approximately 2.73V at 0°C. Because the LM335 supplies a voltage output, it doesn't require the AD590 circuit's precise, low-TC resistor. Accuracy specs at ±2°C from −10 to +100°C for the lowest grade part, calibrated at 25°C.

The LM335's 2.73V output at 0°C is very close to the typical TSC7126's V^+-to-common voltage, therefore requiring some offsetting of the IN LO adjustment pot to ensure that all units calibrate to zero in a production environment. As with the AD590 circuit, a TSC9491 reference can provide the offset, and because the TSC7126 has differential reference inputs, the 9491 can also provide the reference voltage.

If the untrimmed LM335's accuracy is adequate, calibration similar to that employed for **Fig 5**'s AD590 circuit should suffice. Adjust R_2 until the reference voltage (REF HI to REF LO) equals 1.000V, then adjust R_1 until the room-temperature value is displayed. For more accurate performance, measure the calibration error and adjust the reference accordingly. The improved calibration procedure is similar to that for the AD590, except that the LM335's voltage (rather than current) output makes the calculation simpler.

Another bandgap device, which can be used both as a sensor and a reference, is the TSC9495, also sourced by Precision Monolithics Inc and Micro Power Systems Inc. It produces an accurate and stable 5.00V reference, at the same time bringing out an internal circuit node with an output voltage that linearly varies with temperature. Its power consumption is higher than that of the other sensors, but you can use it in applications requiring high sensitivity within a narrow temperature range.

Fig 7 shows how to interface the TSC9495 to the 7126. The 9495's TEMP pin has an output voltage proportional to absolute temperature with a slope of about 2.1 mV/°K. The operational amplifier provides gain scaling and shifts the TEMP pin's level so that the output is within the A/D converter's common-mode range. Although the 7126 has differential inputs that make the op-amp output's absolute value during calibration unimportant, you must still ensure that the 7126's input common-mode range isn't exceeded at temperature extremes.

The op-amp output-voltage change equals $A(dV_{TEMP})/dT$, where

$$A = \text{AMPLIFIER GAIN} = 1 + \frac{R_5}{R_3 \parallel R_4} = 1 + \frac{R_5 R_3 R_4}{R_3 + R_4},$$

and dV_{TEMP}/dT is the 9495's 2.1-mV/°K temperature sensitivity. For an output of 10 mV/°C, A should equal 3.74. However, you can simplify calibration by adjusting V_{REF} to correct for the actual circuit gain instead of precisely adjusting the LM358's gain.

Calibration of this circuit at room temperature requires four steps. First, with power off and pins 4 and 6 of the 9495 shorted, apply 100.0 mV to LM358 pin 1. Measure and record the voltage at LM358's pin 2. Then,

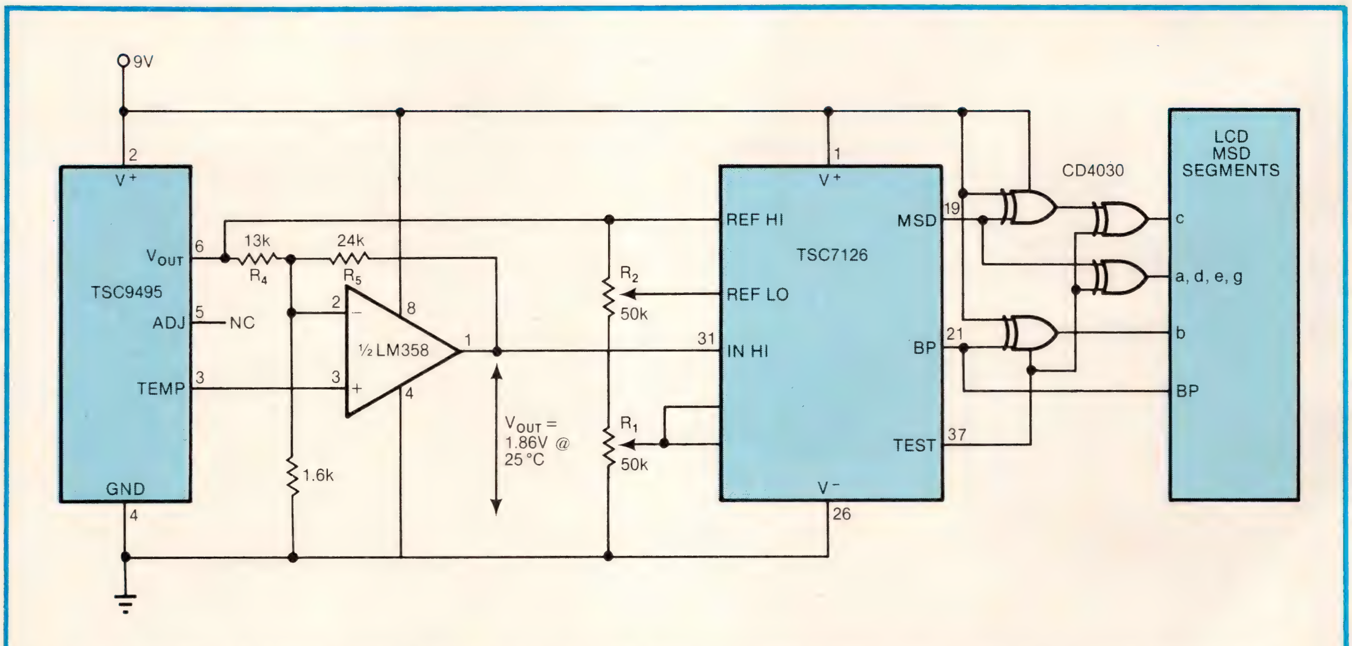


Fig 8—You need a 4-digit display *to use the TSC9495's expanded-scale feature. The MSD output controls the LCD's most significant digit.*

Sensor expands sensitivity over a limited range

remove the short and apply power. Measure 9495's V_{TEMP} and calculate the reference voltage:

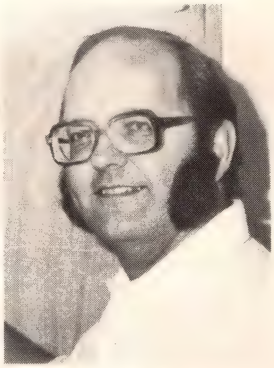
$$V_{REF} = \frac{V_{TEMP} \times 10}{\text{ROOM TEMPERATURE IN } ^\circ K \times V_{PIN\ 2}}$$

Next, adjust R_2 to the calculated reference voltage. Finally, adjust R_1 until the display reads the room temperature.

As noted, the TSC9495 sensor lends itself to expanded sensitivity over a limited range. For example, **Fig** 8's circuit displays temperature from 10.00 to 29.99°C with a sensitivity of 0.01°C/count. Scale expansion can be accomplished simply by changing resistor values; however, you must add logic to the TSC7126 to permit the MSD output to control the display's most significant digit. This configuration, additionally, requires a 4-digit display instead of the 3½-digit unit used in the previously described circuits.

The range of applications of integrating-CMOS-ADC-based thermometers extends beyond digital-readout devices. Other 7000 Series converters provide features that allow you to easily interface them to μPs. Thus, you can use them for temperature-control and data-logging applications while employing the same front-end (sensor) design considerations outlined here. **EDN**

Author's biography



Wes Freeman, applications engineer with Teledyne Semiconductor (Mt View, CA), writes application notes and assists customers with product applications. Before joining Teledyne, he was employed at Precision Monolithics Inc (Santa Clara, CA) in a similar capacity. Wes holds a BS degree in psychology from the University of Illinois. He enjoys competition rifle shooting, photography and home computers in his spare time.

Article Interest Quotient (Circle One)
High **476** ***Medium*** **477** ***Low*** **478**

Design powerful systems with the newest 16-bit μP

Don't be dismayed by the appearance of yet another 16-bit μP; its special features and capabilities, unavailable on its predecessors, make it a prime candidate for inclusion in new system designs.

Robert D Grappel, Hemenway Corp

The introduction of National Semiconductor's 16032 16-bit μP presents system designers with a problem and an opportunity. The problem: Why bother to consider yet another 16-bit μP, perhaps one that lacks software and harbors potential shortcomings, when other, more proven 16-bit μPs are available? The opportunity: The 16032 does indeed provide advantages unavailable in other 16-bit devices. Representing the latest turn in μP evolution, it draws on features of the older machines and adds new capabilities as well. It therefore deserves a close inspection.

By its pinout shall you know it

Fig 1 shows the device's basic signals. Its address bus is 24 bits wide, yielding a 16M-byte linear addressing range (like the Motorola 68000). The data bus is 16 bits wide—as you would expect in a 16-bit μP. The μP's designers have chosen to multiplex these buses in order to fit the μP into a 48-pin package much smaller than the 68000's 64-pin unit.

The 16032's buses are synchronous, using a RDY line to add Wait cycles to accommodate slow memories or I/O devices. This bus structure, familiar to μP-system designers, makes bus interfacing straightforward; most suppliers' interface chips can coexist on it. I/O is memory mapped.

The μP supplies only two interrupt inputs: maskable and nonmaskable (like the Zilog Z8000). External hardware can provide vectored interrupt capability, and the device can support DMA channels and multiprocessor systems. Like the Intel 8086, the 16032 is designed to support closely coupled slave processors, including floating-point (FPU) and memory-management (MMU) devices. It thus generates signals to support these slaves.

One memory-management signal unique to the 16032 is Abort (ABT), which indicates that an instruction has requested an address not available in memory. On the other 16-bit μPs, this action could only result in an error condition. The 16032, however, allows re-execution of instructions; it's the first 16-bit μP to fully support virtual memory, so after the appropriate region of memory has been loaded, it can redo the aborted instruction, picking up exactly where it left off. No registers are changed, and the condition codes are preserved. No other currently available 16-bit μP has this capability.

Register set mixes old and new

As shown in **Fig 2,** the 16032's register complement divides into three classes: general, dedicated and slave. The device has eight 32-bit general registers, which may hold data or addresses interchangeably. They can accommodate byte, word or double-word data, and even/odd register pairs can hold quad-word (64-bit) data. (Among the current crop of 16-bit μPs, only the Z8000 has this capability.) Any general register can also serve as an index or pointer.

(Every rule has its exception, though: The 16032 violates its general-register set's generality in its string instructions, which use registers R_0 through R_4 in a dedicated manner to be described later.)

The μP's dedicated-register set contains six 24-bit and two 16-bit units. The 24-bit registers are all memory pointers. The PC (program counter) is a standard register in all computers, and the μP furnishes two stack-pointer registers, one used in User mode and the other in System mode and during interrupt handling. (A third stack pointer functions during instruction execution, but this action is trans-

Abort signal allows instruction re-execution

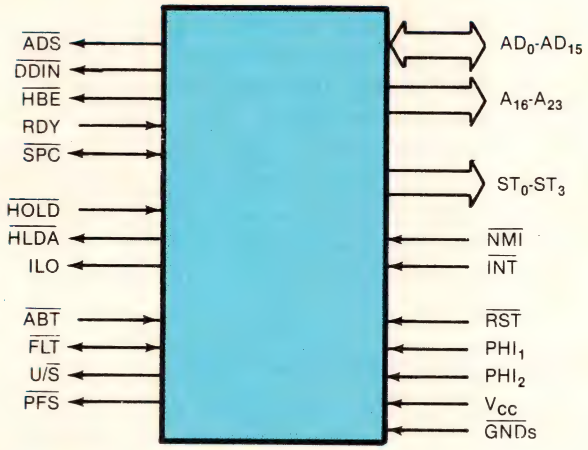
parent to the programmer.)

The presence of two other dedicated registers, the static base (SB) and frame pointer (FP), illustrates the current attitude of μP designers toward high-level languages. These registers provide the functions needed to implement block-structured languages such as PASCAL, C and ADA. The SB register, for example, points to the start of global data for a program module; specifying all data references relative to this register makes programs readily relocatable. The FP register, on the other hand, points to the stack frame for the current program module. Sometimes termed the activation record, this stack frame contains the parameters for the currently executing subroutine and also its local (as opposed to global) variables. To further capitalize on the SB and FP registers, the 16032 has special instructions for easy construction of procedures, blocks, modules and other high-level constructs.

The location of the table of interrupt vectors is fixed in most μPs, usually in low memory. But the 16032 (like the Z8000) provides a dedicated register that contains a pointer to the start of the interrupt-vector table, permitting easy modification of interrupt vectors to suit different needs, simply by moving the pointer.

Fig 3 shows the μP's arrangement of interrupt vectors. Note the traps for the slave processors (FPU, ABT) as well as traps for supervisor call (SVC), conditional trap (FLG), breakpointing (BPT) and tracing (TRC). As on the Z8000, there's only one SVC trap, so software must perform any required vectoring in the system code. The vectored interrupts get generated if you provide additional hardware.

The status register, another dedicated unit, is a standard μP feature. And as in most 16-bit μPs, this 16-bit PSR has a user and a privileged part in the 16032. Status bits for the usual arithmetic conditions allow signed and unsigned comparisons, and a System/User bit indicates the current operational state. You also get bits to control program tracing and one to mask the maskable-interrupt trap; yet another PSR bit flags



BUS

AD_0-AD_{15} — MULTIPLEXED ADDRESS/DATA LINES
A_{16}-A_{23} — ADDRESS LINES
ST_0-ST_3 — PROCESSOR STATUS LINES

INTERRUPTS

$\overline{NMI}$ — NONMASKABLE INTERRUPT
$\overline{INT}$ — MASKABLE INTERRUPT

CHIP CONTROL

$\overline{RST}$ — RESET: INPUT LINE THAT INITIALIZES THE CPU
PHI_1, PHI_2 — 2-PHASE CLOCK INPUTS
V_{CC} — 5V POWER
GNDs — GROUND PINS (2)

BUS CONTROL

$\overline{ADS}$ — ADDRESS STROBE: OUTPUT LINE THAT INDICATES AN ADDRESS HAS BEEN PLACED ON THE BUS

$\overline{DDIN}$ — DATA DIRECTION IN: OUTPUT LINE THAT INDICATES DATA DIRECTION FOR DATA-BUS BUFFERS

$\overline{HBE}$ — HIGH-BYTE ENABLE: OUTPUT LINE THAT ENABLES WRITES INTO THE HIGH-ORDER BYTE OF THE DATA BUS

RDY — READY: INPUT LINE THAT INDICATES THAT THE CPU SHOULD ENTER A WAIT STATE

$\overline{SPC}$ — SLAVE PROCESSOR CONTROL: INPUT/OUTPUT LINE USED IN CPU/SLAVE-PROCESSOR COMMUNICATION

DMA/MULTIPROCESSING

$\overline{HOLD}$ — HOLD: INPUT LINE THAT INDICATES A DMA REQUEST

$\overline{HLDA}$ — HOLD ACKNOWLEDGE: OUTPUT LINE THAT INDICATES ACKNOWLEDGE OF DMA REQUEST

$\overline{ILO}$ — INTERLOCKED OPERATION: OUTPUT LINE THAT INDICATES THAT NO INTERLOCKED TRANSFERS FROM OTHER CPUs ARE TO TAKE PLACE.

MEMORY-MANAGEMENT SUPPORT

$\overline{ABT}$ — ABORT: INPUT LINE THAT INDICATES TO THE CPU THAT THE PRESENT INSTRUCTION WILL BE RE-EXECUTED

$\overline{FLT}$ — FLOAT: INPUT LINE THAT IS USED DURING ADDRESS TRANSLATION MODE TO FLOAT THE CPU OFF THE BUS. IF ADDRESS TRANSLATION IS NOT USED, FLT BECOMES THE DATA STROBE OUTPUT.

$U/\overline{S}$ — USER/SUPERVISOR: OUTPUT LINE INDICATING WHETHER THE CPU IS IN USER OR SUPERVISOR MODE

$\overline{PFS}$ — PROGRAM FLOW STATUS: OUTPUT LINE THAT INDICATES EVERY INSTRUCTION COMPLETION

Fig 1—Hardware signals *provide insight into the 16032's workings.*

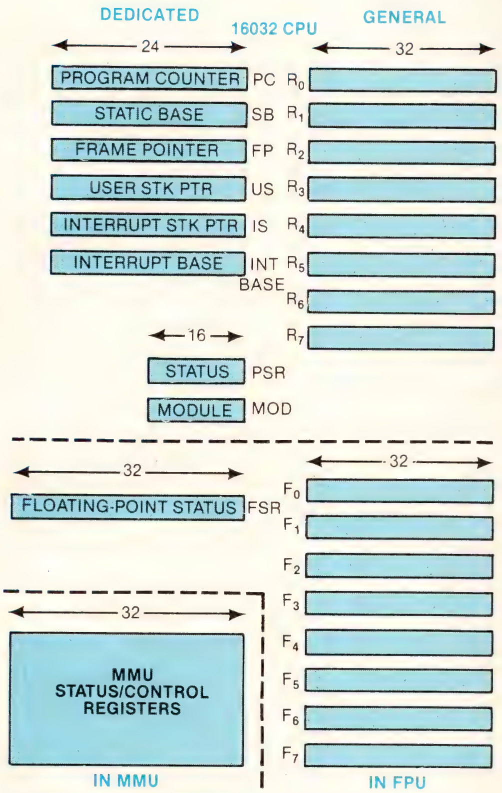


Fig 2—Register architecture *of the 16032 reveals a rich register set. The dedicated registers, in particular, embody concepts not found in other 16-bit μPs.*

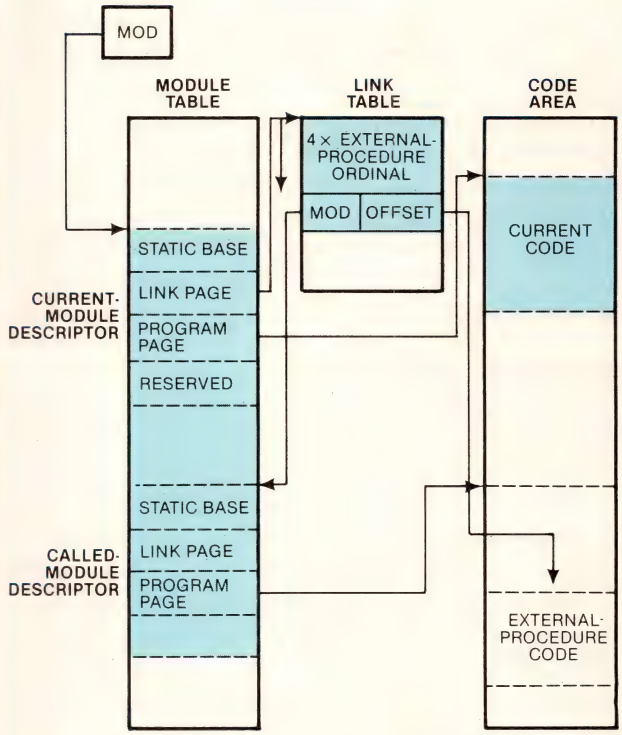


Fig 4—A mechanism for building programs from independent ROMed modules *is inherent in the 16032. The hardware takes care of linking modules.*

various software conditions and can cause traps or branches upon execution of certain instructions.

MOD register—a new idea in μPs

The 16032's 16-bit module-pointer register (MOD) is unique among 16-bit μPs; it simplifies the task of producing truly independent ROMable software modules. The idea that programs should comprise separate, isolated packages is gaining great favor among language designers, and the 16032 is one of the first μPs to provide hardware to facilitate this design strategy.

NUMBER	MNEMONIC	NAME
0	NVI	NONVECTORED INTERRUPT
1	NMI	NONMASKABLE INTERRUPT
2	ABT	ADDRESS-TRANSLATION TRAP
3	FPU	FLOATING-POINT-ERROR TRAP
4	ILL	ILLEGAL-INSTRUCTION TRAP
5	SVC	SUPERVISOR-CALL TRAP
6	DVZ	DIVIDE-BY-ZERO TRAP
7	FLG	FLAG TRAP
8	BPT	BREAKPOINT TRAP
9	TRC	TRACE TRAP
10	UND	UNDEFINED-INSTRUCTION TRAP
11–15		RESERVED
16 +		VECTORED INTERRUPTS

Fig 3—Interrupt structure *of the 16032 is similar to that of other 16-bit μPs.*

Consider, for example, the memory diagram shown in **Fig 4.** Here, the MOD register points to a 16-byte block of memory, a module descriptor. Each such descriptor consists of four addresses: a static base, a link page, a program page and an unused field. The static base is the value that gets stored in the SB register when the module is executed, the program page is the starting address of the module's code, and the link page is a pointer to another data structure, the link table, which gets built by the development software and contains a 32-bit pointer entry for each external reference the module makes. (An entry might be a pointer to actual memory or one to another module descriptor, as shown.)

A module that must call an external module need only know the offset from the start of its link table to the appropriate pointer. The 16032 uses this pointer to update MOD to point to the new module descriptor. The SB register gets updated; the location at which to start

execution is the sum of the new module's program page and the offset in the link-table entry. Returning from the called module reverses these steps, resetting MOD and SB. A specific address mode and special procedure-call and -return instructions provide easy ways to use this facility.

The entire procedure has only one drawback. Because MOD is a 16-bit register, the module table must reside in the first 64k bytes of memory. In addition, because each module descriptor is 16 bytes long, a maximum of 4096 modules may reside in the table. However, this seems a small price to pay for the power the procedure provides.

Every good μP needs slaves

One other dedicated register exists in the 16032—the 4-bit CFG (configuration), not shown in **Fig 2.** Bits in this register notify the 16032 whether its slave processors (FPU, MMU, interrupt controller (IMU), user slave) are installed. These slaves act as extensions to the μP's instruction set and may be installed at any time. In this respect, they're like the Intel 8087 and 8089 coprocessors and the Zilog and Motorola MMUs. To inform the 16032 that the slave instructions should be honored and sent to their respective slave processor, you merely set the appropriate bits in CFG.

Each slave has its own register set, which complements the 16032 set. For example, the FPU has eight 32-bit registers that can hold 32-bit floating-point values or be used in even/odd pairs to hold 64-bit floating-point values. The FPU also has its own status register. The FPU instruction set includes basic arithmetic functions as well as conversions and rounding operations. Attempting to use instructions for a slave processor when it's not installed causes undefined-instruction traps. Use of the CFG register allows easy upgrading of 16032 systems as slave processors become available.

The 16032 steals a page from the 8086's book by encoding its instructions in byte units, unlike the word-sized instructions of other 16-bit μPs. This approach yields several advantages. For example, code can be tighter, even as instruction sets become more complex. The 16032, like the 8086, has a lookahead-instruction cache that preloads as many as eight bytes ahead of the currently executing instruction; instruction operands thus arrive at the processor predigested. Memory fetches can be overlapped with processing, permitting faster execution without requiring faster memory. In addition, the 16032 doesn't care about operand alignments: Word-sized and larger operands can lie on odd-byte boundaries. There's never any need for pad bytes in data records or to worry about mixing byte-sized data into programs.

Another 16032 feature focuses on instruction-set orthogonality. All 16-bit-μP manufacturers claim this advantage, but in practice, all machines must make compromises in this area. The 16032, however, comes very close to the ideal: Nearly all instructions that require two operands can use two totally general addresses. (The 68000 has a 2-address Move instruction, the 8086 and Z8000 have only special cases.)

Thus, the 16032 has very few special addressing cases (the string instructions are the primary offender). **Fig 5** illustrates the typical structure of a 16032 instruction. Note the two addresses' symmetry, which makes the μP easier to program as well as facilitating efficient code generation from language compilers.

The 16032 provides many data types, and it provides them uniformly across its instruction set. You can manipulate bytes, words, double words and even quad words and can handle bits and bit fields. And with the

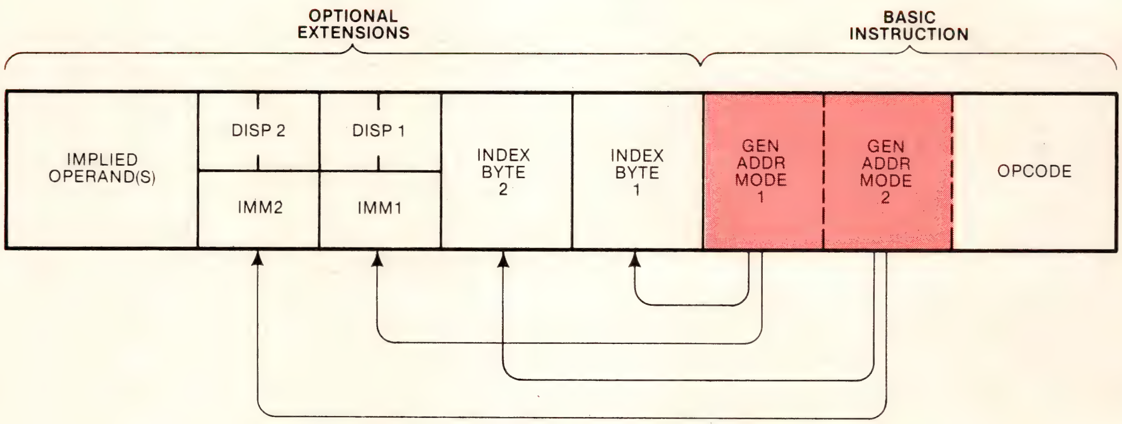


Fig 5—A basic instruction *of the 16032 has two address fields, a unique feature in 16-bit μPs.*

ENCODING	MODE	ASSEMBLER SYNTAX	EFFECTIVE ADDRESS
Register			
00000	Register 0	R_0 or F_0	None: Operand is in the specified register
00001	Register 1	R_1 or F_1	
00010	Register 2	R_2 or F_2	
00011	Register 3	R_3 or F_3	
00100	Register 4	R_4 or F_4	
00101	Register 5	R_5 or F_5	
00110	Register 6	R_6 or F_6	
00111	Register 7	R_7 or F_7	
Register Relative			
01000	Register 0 Relative	disp(R_0)	Disp + Register
01001	Register 1 Relative	disp(R_1)	
01010	Register 2 Relative	disp(R_2)	
01011	Register 3 Relative	disp(R_3)	
01100	Register 4 Relative	disp(R_4)	
01101	Register 5 Relative	disp(R_5)	
01110	Register 6 Relative	disp(R_6)	
01111	Register 7 Relative	disp(R_7)	
Memory Space			
11000	Frame memory	disp(FP)	Disp + Register; "SP" is either SP_0 or SP_1, as selected in PSR
11001	Stack memory	disp(SP)	
11010	Static memory	disp(SB)	
11011	Program memory	disp(PC)	
Memory Relative			
10000	Frame memory relative	disp2(disp1 (FP))	Disp2 + Pointer; Pointer found at address Disp1 + Register. "SP" is either SP_0 or SP_1, as selected in PSR.
10001	Stack memory relative	disp2(disp1 (SP))	
10010	Static memory relative	disp2(disp1 (SB))	
Immediate			
101000	Immediate	value	None: Operand is input from instruction queue
Absolute			
10101	Absolute	@disp	Disp
External			
10110	External	EXTERNAL (disp1) + disp2	Disp2 + Pointer; Pointer is found at Link Table Entry number Disp1
Top of Stack			
10111	Top of Stack	TOS	Top of current stack, using either User or Interrupt Stack Pointer, as selected in PSR. Automatic Push/Pop included
Scaled Index			
11100	Index, bytes	mode[Rn:B]	Mode + Rn
11101	Index, words	mode[RN:W]	Mode + 2 × Rn
11110	Index, double words	mode[Rn:D]	Mode + 4 × Rn
11111	Index, quad words	mode[Rn:Q]	Mode + 8 × Rn "Mode" and "n" are contained within the Index Byte
10011	(Reserved for Future Use)		

Fig 6—Addressing *on the 16032 can take many forms. Some of the modes are standard in all 16-bit μPs, while others are unique to the 16032.*

FPU slave installed, you can use short and long floating-point values as part of the instruction repertoire. Furthermore, you can build and address strings and arrays of these primitive data types.

A multitude of addressing modes

Beyond the register architecture, a μP's addressing-mode complement determines how easily it can be programmed. In this regard, the 16032 provides a remarkably rich set of addressing modes **(Fig 6).** Its Register, Register Relative and Immediate modes are standard features, found in all modern μPs. The Memory Space modes allow use of the new dedicated registers (FP, SB), as well as facilitate position-independent and re-entrant programming (using the SP and PC registers).

The μP's Memory Relative modes provide true indirect-addressing power, a feature lacking in most other μPs. An Absolute mode implements addressing anywhere in memory. And the External mode uses the data structures (module table, link table) previously described to access data items from external modules; the calling program need only know the table-entry number in its own link table to indirectly reference an entry in another module.

The TOS (top-of-stack) addressing mode facilitates the stack-oriented operations typical of languages such as PASCAL, C and ADA. Effectively, a Read operation using TOS addressing is a Pop, while a Write is a Push.

The Scaled Index mode, finally, is unique to the

16032; it provides automatic indexing of arrays whose data items are bytes, words, double words or quad words. The 16032 even extends the idea of a displacement; in this μP, a displacement may be one, two or four bytes long—the length is actually encoded into the displacement itself. Byte displacements always have a zero in their high-order bit, even if the displacement is negative. Thus, they can range from −64 to +63. Word or double-word displacements always have their high-order bit set, even if positive; the next bit indicates the length of the displacement. This mechanism allows a displacement to be only as long as necessary to address its operand. The entire address space can be reached by a displacement from any register. (Compare this feature with its equivalent in the 68000, whose 16-bit displacements limit indexing to a 64k-byte range.) Displacement length is decoded during the prefetch of the instruction bytes and thus exacts no performance penalty.

An example clarifies instruction-set power

An example of a 16032 instruction illustrates the power of the μP's instruction set. Note first that an instruction can be a single byte or contain more than 20 bytes; the encoding can thus become quite complicated. Then consider the following instruction:

MOVMD 4(−8(FP)),16(R_1)[R_3:W],8

This instruction moves blocks of data from one address to another. Suppose you want to move eight double words. The source address is Memory Space relative, using the FP register, while the destination is Scaled Index, using R_3 as the index into a word-size array. The array's base address is specified using Register Relative addressing from R_1. To begin, all block instructions start with the byte CE_H; this Escape byte indicates that the following byte begins the actual instruction. The basic instruction is then encoded as

10000	11101	0000	11	11001110	
(FP)	[Rn:W]	MOVM	D	block instr	8743CE

The next byte gives the destination mode, which indicates R_3 as index and R_1 relative as the base mode. This encodes as $4B_H$. The instruction is now four bytes long: 4B8743CE. The next byte is the source mode displacement 1. This is −8; encoded for a byte displacement, it's 78_H. And the next byte is the source mode displacement 2—04_H. The instruction has now grown to six bytes: 04784B8743CE. Next comes the destination—10_H. Finally, you need the final instruction operand, the count of 08_H. The final instruction is therefore eight bytes in length: 081004784B8743CE. Larger displacements could make it still longer.

A mode is missing

After this discussion, you might think the 16032 provides every addressing mode a programmer could want. Unfortunately, two modes are missing—the Autoincrement and Autodecrement modes found on the 68000. The TOS mode can serve in many of the cases where you might use these two modes, but it only works off the dedicated stack pointer. Thus, there's no clean way to implement multiple stacks, which prove useful in implementing languages such as FORTH or in coding expression evaluators or macro processors.

Then, too, although the block and string instructions provide autoincrement and autodecrement capability, for them the 16032's instruction set loses its symmetry. However, this is certainly not a critical deficiency; other 16-bit μPs don't have these modes, either.

Instruction set provides extensive capabilities

The 16032 has an extremely extensive instruction set. Consider some of the most noteworthy and useful of these instructions.

The μP's arithmetic capabilities, for example, are impressive. Add, subtract, multiply and divide are supported for all data sizes from byte to double word. And extended arithmetic instructions permit division of a quad word by a double word and multiplication of two double-word operands to produce a quad-word result. Only the Z8000 also provides this capability.

The 16032 also has an absolute-value instruction, and you get signed and unsigned division instructions and signed and unsigned remainders. Furthermore, instructions to add and subtract packed-decimal (BCD) values of any length from byte to double word are part of the set, going beyond the capabilities of other 16-bit μPs. Logical instructions include AND, OR, XOR, NOT and BIC; the last is the AND of the destination with the complement of the source. Sign-extend and zero-extend instructions are provided, and a family of "quick" instructions permits tighter encoding of instructions using small constants. Finally, if you add the FPU chip to the system, the 16032 furnishes a complete set of floating-point instructions on both single- and double-precision operands.

The μP's bit-manipulation instructions are the most extensive of any currently available μP. The key to their use is that a bit may be addressed as an offset from a base address anywhere in memory; the 16032 automatically finds the byte that contains the addressed bit and extracts that bit. You can test, clear, set and invert bits; the Clear Bit and Set Bit instructions have the indivisible forms required in multiprocessor-synchronization programs (test and clear, test and set). A particularly noteworthy bit instruction is Find First Set Bit, which permits scanning a bit field while counting the number of cleared bits. This instruction proves useful wherever you use bit arrays.

The field instructions, unique to the 16032, permit

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Byte-sized instructions increase code compactness

easy manipulation of such arrays, such as PASCAL's Set construct or bit maps of memory or disk allocation. Fields consisting of a bit array can be extracted and inserted on arbitrary "bit" boundaries; a field can span one to 32 bits. These fields are always right justified after extraction, and any unused bits in the destination operand get cleared.

Although string instructions are a part of the instruction sets of other μPs, the 16032 extends them to virtual subroutines in a single instruction. Indeed, the only drawback to the 16032's string instructions is that they use registers R_0 through R_4 in a dedicated manner:

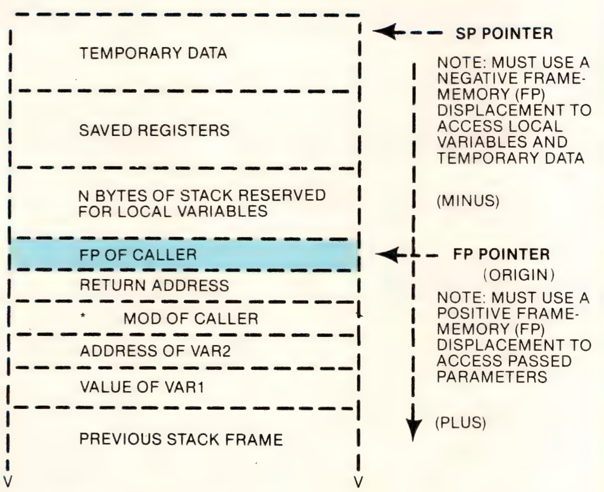
- R_0: Number of items in the string(s)
- R_1: Address of origin of first string
- R_2: Address of origin of second string (if needed)
- R_3: Address of origin of translation table (if needed)
- R_4: Termination value (if needed).

Strings can consist of data items ranging from bytes to double words. (You can only use translation for byte strings.) And you can scan them forwards or backwards. You can also specify a translation table to convert a string's byte value to a table entry indexed by the byte. Furthermore, you can specify a While/Until condition, which compares the string element accessed (with possible translation) with the value in register R_4. This instruction continues so long as the element matches R_4 (While), or so long as it does not match (Until). String instructions also terminate when their count (R_0) decrements to zero, and strings can be moved, compared and scanned.

As an example of the power of these instructions, consider the task of moving to a buffer a string as long as 256 characters. In this operation, lower-case characters should be converted to upper case, and movement should stop when the program finds a character that's not a letter, digit or dollar sign. Assuming an appropriate translation table, this entire operation requires just one 16032 instruction.

Because they are so powerful, the 16032's string instructions are made interruptible. Thus, an interrupt can be serviced during execution of a string instruction; it doesn't disturb the string operation, which resumes at the point where it was interrupted.

Block instructions allow moving and comparing data items as long as 16 bytes in one step. These instructions use two addresses instead of the dedicated registers of the string instructions.



*SAVED PSR ON EXCEPTIONS
UNUSED IN PROCEDURE CALLS
ITS LENGTH, 2 BYTES, IS COMPENSATED
FOR AUTOMATICALLY BY THE PROCEDURE CALLS

Fig 7—Procedure invocations *use a stack frame to hold local variables, parameters and other information. The 16032 provides special instructions and facilities for building and manipulating stack frames.*

μP thinks like a high-level language

Illustrating the trend to the use of high-level languages (HLLs), the 16032 provides instructions that implement HLL constructs. Along with the dedicated registers MOD, FP and SB and the Scaled Index addressing mode, these instructions permit an assembly-language programmer to think and produce code at a higher level than that accommodated by other μPs.

The Index and Check instructions, for example, permit easy and straightforward addressing of multidimensional arrays of any data type. Check performs two operations. First, it checks that an index register lies between an upper and lower bound, specified as a pair of constants in memory and of any standard data length. Second, it adjusts the index register by subtracting the lower bound from that register. Hence, it automatically adjusts the index's origin.

Index performs one step of the array-address calculation. Specifically, the specified register gets multiplied by the size of the array dimension and then added to the index value. As an example, consider IARRAY, an array of 32-bit integers with three rows and four columns. Suppose you wish to perform this operation:

IARRAY(I,J):=1

On the 16032, you do it with six instructions:

```
CHECKD R0,BOUND2,J     check second dimension
FLAG                   trap if out of range
CHECKD R1,BOUND1,I     check first dimension
FLAG                   trap if out of range
INDEXD R0, 3, R1       compute array index
MOVD 1, IARRAY [R0:D]  store value
```

BOUND2 is the address of a pair of 32-bit constants: 1 and 4. Similarly, BOUND1 denotes constants 1 and 3. Note that you could perform this operation in only three

Auctoincrement and Autodecrement modes aren't available

```
            PASCAL
MODULE DELAY;
EXPORT OLDT: INTEGER;
EXPORT PROCEDURE ADDTO(VAR T: INTEGER; N: INTEGER);
VAR
    TEMP: INTEGER;
BEGIN
    TEMP := OLDT;
    OLDT := T;
    T := TEMP + N;
END.
        NS16000 ASSEMBLY
        .PROGRAM
        .EXPORT ADDTO,OLDT
ADDTO:  ENTER    [R7],4            ;save R7 and allocate space for TEMP
        MOVD     16(FP),R7         ;get address of T into R7
        MOVD     0(SB),-4(FP)      ;move OLDT into TEMP
        MOVD     0(R7),0(SB)       ;move T into OLDT
        MOVD     -4(FP),0(R7)      ;move TEMP into T
        ADDD     12(FP),0(R7)      ;add N to T
        EXIT     [R7]              ;restore R7, discard TEMP and restore FP
        RXP      8                 ;return and remove T and N from stack
        .ENDSEG
        .STATIC
OLDT:   .BLKD    1
        .ENDSEG

    PASCAL
PROGRAM TEST(INPUT, OUTPUT);
IMPORT DELAY;
VAR
    T: INTEGER;
BEGIN
    OLDT := 0;
    T := 0;
    ADDTO(T, 3);
END.
        NS16000 ASSEMBLY
        .PROGRAM
        .IMPORT OLDT
        .IMPORT ADDTO
TEST:   MOVQD    0,EXTERNAL(0)     ;move 0 into OLDT
        MOVQD    0,0(SB)           ;move 0 into T
        ADDR     0(SB),TOS         ;push address of T
        MOVQD    3,TOS             ;push 3
        CXP      ADDTO             ;call ADDTO
        SVC                        ;return to operating system
        .ENDSEG
        .STATIC
T:      .BLKD    1
        .ENDSEG
```

Fig 8—When converting PASCAL to 16032 instructions, *the 16032 allows a compiler to generate very compact and logical code.*

instructions if you omit the boundary-checking steps.

The 16032 also provides an instruction that implements the HLL Case statement. Suppose register R_1 contains a word between 0 and 4 and you wish to jump to one of five addresses depending on this value. You would code the operation as follows:

```
L1: CASEW T1[R1:W]     case instruction
T1: .WORD L1-label0    where to go if R1=0
    .WORD L1-label1                   1
    .WORD L1-label2                   2
    .WORD L1-label3                   3
    .WORD L1-label4                   4
```

A Check should precede Case to trap out-of-range values and to adjust for ranges not starting with zero.

Accommodating activation records

As noted previously, the 16032 provides instructions to enter and exit a context; these instructions combine the functions of several instructions in other μPs. ENTER, for example, pushes the FP onto the stack, adjusts the stack pointer to provide space for local variables and pushes the specified general registers onto the stack. The FP gets updated to point to the local variable space. EXIT reverses this process,

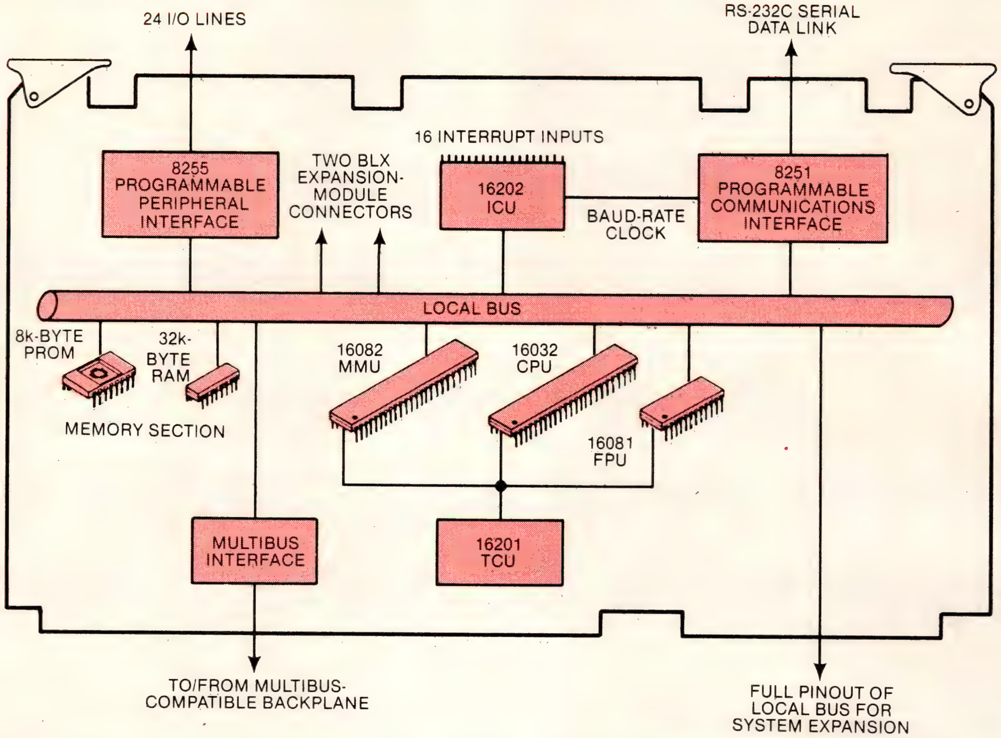


Fig 9—A μP needs support, *and National's DB16000 board provides it on a Multibus-compatible card. Support is also available for the floating-point (FPU) and memory-management (MMU) units soon to become part of the 16000 family.*

restoring the saved registers and the FP while reclaiming the stack space used by the local variables. The Return instructions provide for adding a constant to the SP upon return; this procedure furnishes a way to remove passed parameters from the stack.

Also as noted earlier, the 16032 provides instructions to call and return from external procedures. These CXP and RXP instructions maintain the MOD and SB registers as well as return addresses. For example, consider the following external-procedure invocation, in which two parameters get passed, one by value and a second by address:

```
      MOVD var1,TOS    param 1 value to stack
      ADDR var2,TOS    param 2 address to stack
      CXP name         call procedure
```

The body of the procedure is:

```
name:  ENTER [reglist],n   n bytes of local variables
       .....
       .....
       EXIT [reglist]      restore stack frame
       RXP  8              eight bytes of parameters
```

Fig 7 shows the stack-frame organization produced by this example. Note how closely this operation parallels the working of block-structured languages.

Fig 8 shows the instructions a PASCAL compiler for the 16032 might generate, given a main program TEST calling on an external procedure ADDTO. Each module has a global variable (T in TEST and OLDT in ADDTO) which gets accessed via the SB register. Module ADDTO has a local variable TEMP, accessed using the FP register. (Note the use of "quick" instructions in TEST to move the constants 0 and 3.) ADDTO illustrates the 2-address ADD instruction. Two parameters get passed to ADDTO using the previously described framework. (Note also the use of External addressing in TEST to access a variable in ADDTO.)

"Fine," you say, "the 16032 sounds great on paper. But how do I get to use it?" To answer this question, National provides the DB16000 single-board computer. Much more than the usual evaluation board, this Multibus-compatible card is a powerful computer in its own right. **Fig 9** shows its block diagram; the 16032 μP combines with its clock-generator chip (16201 TCU), which provides timing for all other devices on the board and handles such functions as Wait-state generation and reset shaping.

The board also includes 8k bytes of EPROM, which store a monitor/debugger. A few simple jumper changes accommodate an additional 8k of PROM. In addition, the standard board comes with 32k of RAM; exchanging the 16k RAMs for 64k devices and making some jumper changes expands this figure to 128k.

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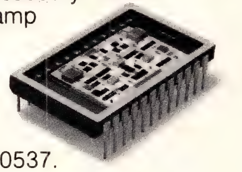

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Evaluation board provides full computer support

hardware. Board memory is dual ported—a feature missing from some Multibus processor boards. An 8255 provides parallel I/O capabilities, complete with driver chips (7437s), and an 8251 drives a serial line for the monitor/debugger terminal. You can add additional serial and parallel I/O directly on the local bus, using the two expansion connectors provided.

As parts become available, you'll be able to add the 16202 interrupt controller (ICU) to the DB16000, providing support for the eight Multibus interrupt lines and eight more interrupt inputs. The ICU will also contain two programmable timers, one of which the DB16000 will use as a baud-rate generator for the 8251. (Boards shipped without ICUs have a fixed baud rate of 9600.)

The DB16000 also provides a socket for the 16081 FPU, which you'll be able merely to plug in when it becomes available. A socket and support for the 16082 MMU is also provided.

The monitor provides a rich set of commands. A Transparent mode permits use of the board with a separate development system: Upload and Download commands permit transfer of programs and data between the development machine and the board. Local mode includes commands to display and modify every register of the 16032 and the FPU and MMU slave processors. And memory-change, -fill and -search commands make it easy to work with programs in the DB16000's memory. Debugging can occur via Breakpoint and Trace commands, and Step-While and Step-Until provide a flexibility in specifying break conditions seldom found in this type of computer. Finally, if you install the MMU, you can bring its debugging facilities to bear on a problem.

As an additional very nice point, National supplies the complete source code of the monitor. Basic I/O routines are directly callable, and their calling conventions are clearly specified—providing you with a good start toward understanding how to code for the device.

In sum, the 16032 seems to be a powerful and well-designed processor. Its instruction set contains features available on no other single μP, and its capabilities will increase dramatically as its slave processors become available. The DB16000 board is a practical and useful way to test out this newest of the 16-bit μPs. **EDN**

Author's biography

Robert Grappel is vice president of Hemenway Corp, a Boston, MA software-systems supplier.

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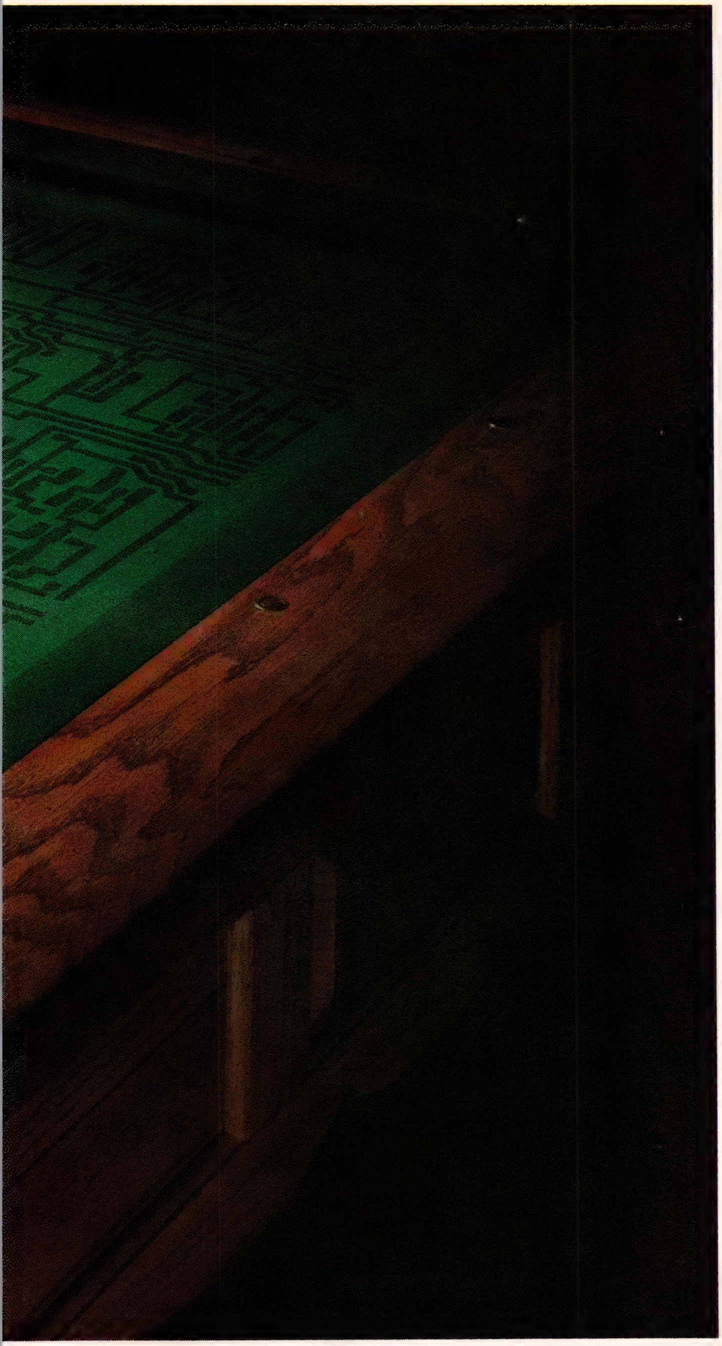

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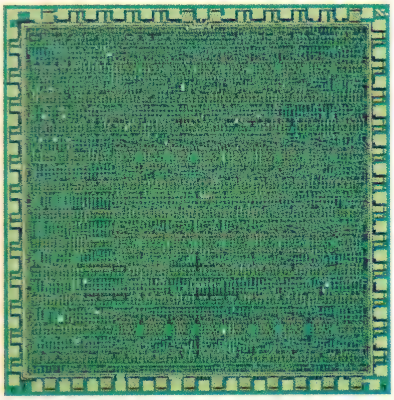

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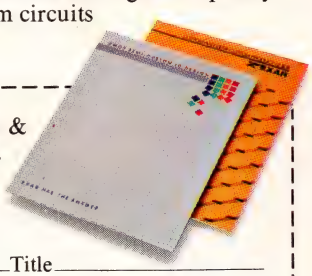

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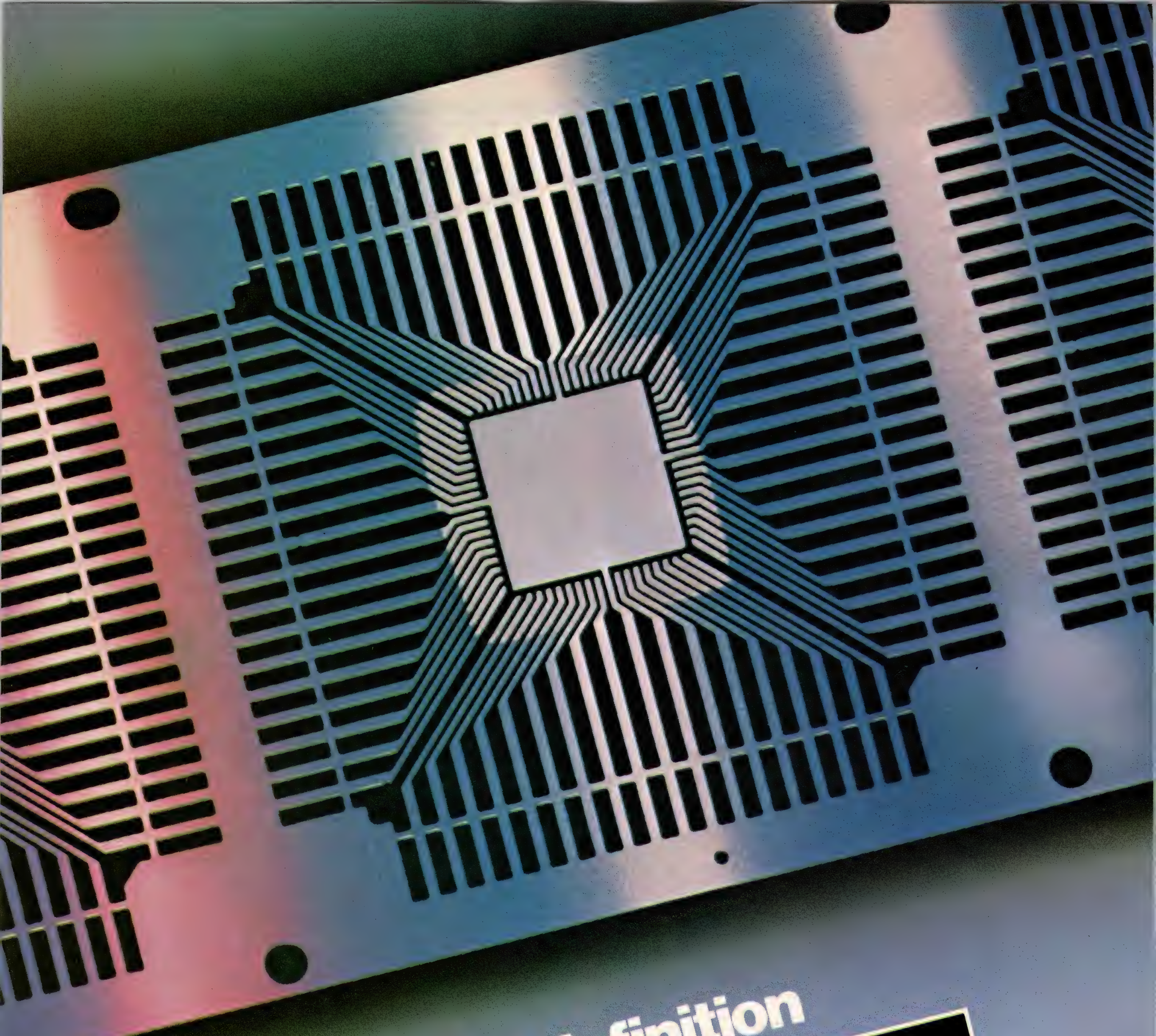


Multitasking-PASCAL extensions solve concurrency problems

Deadlocks and indefinite postponements threaten any multitasking environment. Task-synchronizing extensions to multitasking PASCAL defeat these threats.

Peter H Mackie, Interactive Technology Inc

To avoid deadlock (one process waiting for a resource that another process can't release) and indefinite postponement (one process being continually denied a resource request) in your multitasking-system application, you can use a high-level development language with built-in concurrency handlers. Parallel PASCAL is one such language; it extends standard PASCAL via special task synchronizers: a new data type called Signal, new system procedures called Wait and Send and a Boolean function termed Awaited. To understand the language's use, examine the problems it helps solve.

System deadlock brings operations to a halt

Multitasking programming poses difficulties not present in sequential programming. In multitasking, different processes require shared system resources; therefore, programmers can't anticipate potential conflicts between simultaneous tasks. One of the most devastating possibilities, deadlock, results because no process can gain access to an assigned resource until the controlling process releases that resource.

Deadlocking (**Fig 1**) can occur when a process holds resources while requesting others it needs to perform a function. It can't release the held resources until it completes the function. But the required resources might be similarly monopolized by a likewise stymied process. Thus, two or more processes can wait forever for delivery of the needed resources.

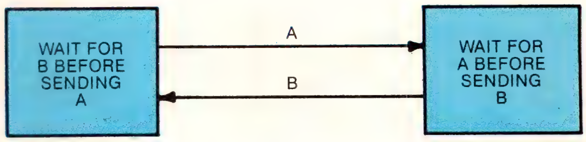


Fig 1—Deadlock occurs *when tasks hold on to needed system resources while requesting others.*

If deadlock occurs, system functions stop. Clearly, multitasking programs performing process control, monitoring or handling must supply some method of resource management that averts deadlocking.

The classical problem of the dining philosophers (**Fig 2**) illustrates the potential for deadlock and one method of eliminating that potential. In this multitasking analogy, five philosophers spend all of their lives doing one of two things: eating or thinking. Each philosopher has a large plate of spaghetti and a place at a table. To eat the spaghetti, each philosopher needs two forks. However, each philosopher initially has only one fork—a total of five are thus available. The philosophers won't ever be able to eat unless they share their forks, and each can only share forks with his neighbors to his immediate right and left. The problem is to simulate the processes of alternately eating and thinking while avoiding deadlock (ie, a philosopher holding one fork never being granted the request for the other). Because each philosopher must pick up and put down forks independently of all the others, and because each can potentially monopolize a system resource (fork) required by another, the problem provides a good analogy for concurrency handling in multitasking process control.

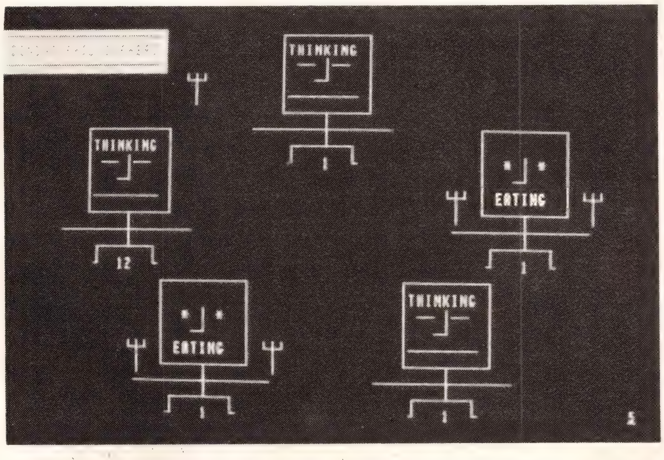


Fig 2—The dining-philosophers problem *illustrates the deadlock potential inherent in a multitasking system. Each philosopher must share forks with adjacent philosophers but needs two forks to eat. If philosophers get locked out of one or both forks, they starve.*

How can the philosophers eat and think while avoiding deadlock? Note that with only five forks available, only two philosophers can eat at one time.

Five dining philosophers symbolize multitasking

And because only neighbors can share forks, no two adjacent philosophers can eat at the same time.

A straight-ahead, intuitive solution has each philosopher, in parallel with all the others, execute a process of picking up forks, eating, putting down the forks and thinking **(Fig 3)**. In this too-simple solution, each philosopher concurrently invokes Pickup and Putdown procedures to access and release the forks, first left and then right, with the fork index passed as a parameter. The procedures can use a Boolean array, Fork Free[I], to discern the availability of fork I. Only after acquiring two forks can a philosopher stop thinking and start eating. Within these constraints, eating and thinking functions can call a Pause to generate random durations.

Unfortunately, in this innocuous solution lies a potential deadlock situation: Everything would continue smoothly until no philosopher can complete a Pickup procedure because of an eternally unavailable fork. What happens, for instance, when each philosopher, in parallel, picks up a left fork and attempts to acquire a right one? Very rapidly, each philosopher blocks another's Pickup procedure by holding one fork and waiting for one held similarly by another. Deadlock then occurs because processes (philosophers) hold certain resources while requesting others. The philosophers, if they are to eat, need a better solution.

Consider a more involved program, one that doesn't rely on a process's holding only part of the resources needed for a task **(Fig 4)**. Now the philosopher process employs a parameter, I, corresponding to an index number (1 to 5) for the various philosophers. More important, the acts of picking up and putting down forks now consist of single procedures, with the philosophers' index as the parameter. If the programming language permits tasks to signal each other concerning the availability of resources, each philosopher can wait until two forks become available before executing the Pickup procedure. Causing a task to wait in this manner before monopolizing resources thus eliminates deadlock.

```
PROCESS PHILOSOPHER;
BEGIN
 REPEAT
  PICKUP(LEFT);
  PICKUP(RIGHT);
  { Eat for awhile }
  PUTDOWN(LEFT);
  PUTDOWN(RIGHT);
  { Think for awhile }
 UNTIL FALSE;
END;
```

Fig 3—In a straight-ahead, inadequate solution to the deadlock problem, *philosophers execute a process in parallel. If all philosophers picked up left forks simultaneously, each would block another's request for a right fork.*

```
PROCESS PHILOSOPHER(I:INTEGER);
BEGIN
 REPEAT
  PICKUP(I);
  { Eat for awhile }
  PUTDOWN(I);
  { Think for awhile }
 UNTIL FALSE;
END;
```

Fig 4—A better deadlock solution *uses philosopher numbers as parameters. Pickup and Putdown now access and release forks via single procedure calls. With communication between tasks thus provided, a philosopher can only pick up forks when two become available.*

Parallel PASCAL employs extensions that make such intertask communication and synchronization possible (see **box,** "Parallel PASCAL's extensions ease concurrency handling"). In this language, tasks can pass a new data type (Signal), indicating conditions.

Two procedures—Wait and Send—suspend a task or resume a suspended task using a specified Signal variable as parameter. And the Awaited function indicates the existence of tasks waiting on a given signal variable. (You must initialize all signal variables to zero before using them.)

Fig 5 shows the completed solution to the philosophers' deadlock problem, employing the concurrency extensions available in Parallel PASCAL. Pickup and Putdown procedures must use variables to track fork availability, similar to the Fork Free method used in the earlier, inadequate solution. A 5-element array, Myforks[I], holds the number of forks available to philosopher I: 1, 2, 3, 4 or 5. Now the Pickup procedure allows philosopher I to pick up forks only when Myforks[I]:=2. Otherwise, philosopher I waits on the Ready[I] signal variable, sent by another philosopher during Putdown, indicating two available forks. The array Ready[I] signifies that each blocked philosopher waits on his own signal.

When philosopher I succeeds in accessing his two forks, he must decrease the Myforks variable for the philosophers to his left and right. Functions Left[I] and Right[I] index these adjacent philosophers: Left[4]:=3 and Right[4]:=5, for example. Note, too, that the closed philosopher ring means that Right[5]:=1 and Left[1]:=5. On Pickup, then, philosopher I must decrement Myforks[Left[I]] and Myforks[Right[I]].

After successfully completing the Pickup[I] procedure, the philosopher eats for a while. When ready to return the forks, the philosopher calls Putdown[I],

increasing his neighbors' fork counts. If either neighbor's forks count reaches 2, the philosopher signals that neighbor with the appropriate Ready signal. Such communication among the philosophers eliminates all possibility of contention.

Keep errors nonexistent

Errorless concurrency handling requires that nothing happens to a given variable between the time a task tests it and the time the task acts on the test result. In the example, if a philosopher finds two forks available to his neighbor, those forks must still be available when the philosopher sends a Ready signal to the neighbor. In this regard, a segment of code that accesses or tests variables that other tasks must not alter is called a critical region.

Parallel PASCAL protects such critical regions by giving a task full control of the processor until the task executes a Send or Wait. Any code region not containing a Send or Wait is a protected critical region and may test or use system resources without other tasks interfering.

You can keep a region critical with respect to a given resource and still extend it over Sends and Waits by framing it with semaphore procedures. A semaphore record used for this purpose combines two variables, a Boolean and a Signal (**Fig 6a**). A task accessing the critical region sets the Boolean to indicate the region's occupation. A subsequent task, finding the Boolean indicating a task already in the region, must Wait on the semaphore's Signal portion. When the first task leaves the region, it resets the Boolean and sends the Signal, restarting the waiting task. Thus, only one task can enter the critical region at a time. **Fig 6b** shows PASCAL Grab and Release procedures for critical-region management.

Proper concurrency handling also requires that a sent signal still be valid when a task waiting on the signal resumes. Parallel PASCAL ensures this validity by transferring program control to a waiting task immediately after a Send procedure. Because a philosopher receiving a two-forks-ready signal gains immediate program control, that philosopher will therefore still have two forks available when resuming Pickup.

Decreasing indefinite postponement

Turn now to the second problem that a multitasking system must avoid. When a task, while not technically

Parallel PASCAL's extensions ease concurrency handling

Extensions to PASCAL allow Parallel PASCAL to handle multitasking without fatal contention between tasks.

In this language, "process" and "task" have related but distinct meanings. A process is a block of PASCAL code that the compiler translates into a block of machine code. Formally identical to a procedure but using the Process identifier, this process may have parameters and local variables, may call procedures and functions and may declare procedures and functions internally.

Calling a process creates a task; ending a process destroys that task. A task is therefore the dynamic execution of a process. While not truly simultaneous, tasks share the computer so rapidly and smoothly they appear to run at the same time. Each task has a scheduling block linked into a circular list where the processor checks it for execution.

Tasks are either active, eligible or waiting. An active task controls the processor. A waiting task waits for a signal and gains processor control immediately following the signal. When a task gives up the processor after completion or after executing a Wait, the processor moves around the scheduling list on a round-robin basis, executing the next eligible task. (Parallel PASCAL also provides interrupt features that create exceptions to these rules.)

Tasks communicate via a new data type called Signal. You must initialize any signal variables to zero before using them. Procedures Wait and Send use signal variables as parameters. The Wait procedure can have an optional integer parameter called the rank (default value of 1).

After executing a Wait(S, R), a task relinquishes the processor and goes into a queue of tasks waiting for signal S. It goes ahead of all waiting tasks having lower rank and behind all waiting tasks having the same or higher rank (1 is highest). Execution proceeds to the next available task; the waiting task resumes only when it reaches the top of the queue and some other task sends the queue's signal. Read and Write can call Wait implicitly.

The procedure Send(S) suspends the current task and links it into the eligible-task list. The topmost task in the queue of tasks waiting for S begins executing. On an empty queue, execution continues with the sending task. (Sends and Waits in interrupt processes follow slightly different patterns.) The Boolean function Awaited(S) is TRUE if at least one task waits for S, FALSE otherwise. Awaited does not switch tasks.

For more information on Parallel PASCAL, **Circle No 648.**

locked out, can't access all required resources because of a repeating block, indefinite postponement has occurred. For example, if philosopher 1 has just picked up forks and philosopher 3 has just put forks down, philosopher 2 can enter Pickup, find one of the forks busy, and wait. Before philosopher 1 finishes eating, philosopher 3 picks up forks again. Philosopher 1 finishes eating, releases forks, thinks a bit and picks up forks before philosopher 3 releases forks. Philosopher 2 therefore never has two forks available and would starve if the sequence repeated forever.

Reducing the possibility of such postponement involves introducing an age variable for each fork requester and then holding the fork for the oldest requester. An array of signals, Maxwait[I], can continuously identify the longest wait for forks. **Fig 7** shows a Pickup procedure modified in this manner. Now only the longest waiter can complete Pickup. But a philosopher with two available forks can't eat if another has waited longer, even if the latter has no forks available.

This solution reduces parallelism to a minimum. Another solution counts the meals enjoyed by a waiting

```
VAR
I: INTEGER;
MYFORKS: ARRAY[1..5] OF INTEGER;
READY: ARRAY[1..5] OF SIGNAL;

PROCEDURE PAUSE(I:INTEGER);
 { CALLED BY ANY TASK DESIRING A TIMED WAIT }
BEGIN
 WHILE 1 > 0 DO
  BEGIN
   { WAIT FOR A DEFINED PERIOD OF TIME }
   I:=I-1;
  END;
END;{ PAUSE }

FUNCTION RIGHT(I:INTEGER):INTEGER;
{ CALCULATES PROPER RIGHT NEIGHBOR PHILOSOPHER }
BEGIN
 IF I < 5
 THEN RIGHT:=I+1
 ELSE RIGHT:=1;   { RIGHT OF PHILOSOPHER 5 IS PHILOSOPHER 1 }
END;{ RIGHT }

FUNCTION LEFT(I:INTEGER):INTEGER;
{ CALCULATES PROPER LEFT NEIGHBOR PHILOSOPHER }
BEGIN
 IF I > 1
 THEN LEFT:=I-1
 ELSE LEFT:=5;   { LEFT OF PHILOSOPHER 1 IS PHILOSOPHER 5 }
END;{ LEFT }

PROCEDURE PICKUP(I:INTEGER);
BEGIN
 IF MYFORKS[I] <> 2
 THEN WAIT(READY[I]);
                 { WAIT UNTIL BOTH ADJACENT FORKS ARE AVAILABLE... }
 MYFORKS[RIGHT(I)]:=MYFORKS[RIGHT(I)]-1;   { THEN DECREMENT NEIGHBOR }
 MYFORKS[LEFT(I)]:=MYFORKS[LEFT(I)]-1;     { PHILOSOPHER FORK COUNT }
END;{ PICKUP }

PROCEDURE PUTDOWN(I:INTEGER);  { STOP EATING, START THINKING }
BEGIN
 MYFORKS[RIGHT(I)]:=MYFORKS[RIGHT(I)]+1;   { PUT DOWN THE FORKS }
 MYFORKS[LEFT(I)]:=MYFORKS[LEFT(I)]+1;
 {  SIGNAL ADJACENT PHILOSOPHERS IF THEY HAVE THE 2 FORKS AVAILABLE }
 IF MYFORKS[RIGHT(I)] = 2
 THEN SEND(READY[RIGHT(I)]);
 IF MYFORKS[LEFT(I)] = 2
 THEN SEND(READY[LEFT(I)]);
END;{ PUTDOWN }

PROCESS PHILOSOPHER(I:INTEGER);
BEGIN
 REPEAT
  PICKUP(I);
  WRITE(' EATING  ');
  PAUSE(I);
  PUTDOWN(I);
  WRITE(' THINKING');
  PAUSE(I);
 UNTIL FALSE
END;{ PHILOSOPHER }

BEGIN { MAIN }
 FOR I:=1 TO 5 DO  { INITIALIZE THE PROGRAM VARIABLES }
  BEGIN
   MYFORKS[I]:=2;
   READY[I]:=NIL;
  END;{ FOR }
 FOR I:=1 TO 5 DO   { START THE 5 PHILOSOPHER TASKS }
  PHILOSOPHER(I);
END { DINING PHILOSOPERS }.
```

Fig 5—The completed code *integrates the philosopher process into a main routine. Philosophers use the Ready signal to tell their neighbors when one has two forks (held in variable Myforks) free.*

```
         TYPE
            SEMAPHORE=RECORD
               OCCUPIED : BOOLEAN;
               CONTINUE : SIGNAL;
(a)         END;

         VAR
            SEM:SEMAPHORE;
              {Semaphore data type defined in Fig 6a}
         PROCEDURE GRAB;
         BEGIN
            IF SEM.OCCUPIED THEN WAIT (SEM.CONTINUE)
              {Wait here for resource to free up}
            SEM.OCCUPIED:=TRUE;
              {Grab the resource}
         END;

         PROCEDURE RELEASE
         BEGIN
            SEM.OCCUPIED:=FALSE;
              {Release the resource}
            SEND (SEM.CONTINUE);
              {Tell other tasks waiting through a Grab
               that the resource is available}
(b)      END;
```

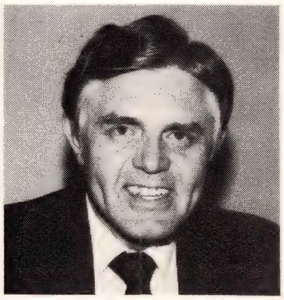
Fig 6—Critical-region management *starts with a semaphore record* ***(a)****, which combines a Boolean and a Signal variable. Grab and Release procedures* ***(b)*** *provide the actual management functions.*

```
PROCEDURE PICKUP(I:INTEGER);
 BEGIN
  WAIT(MAXWAIT[I]);        { WAIT FOR THE LONGEST 'WAIT TO EAT' }
  IF MYFORKS[I] <> 2
  THEN WAIT(READY[I]); { WAIT UNTIL BOTH ADJACENT FORKS ARE AVAILABLE..}
  MYFORKS[RIGHT(I)]:=MYFORKS[RIGHT(I)]-1;   { THEN DECREMENT NEIGHBOR  }
  MYFORKS[LEFT(I)]:=MYFORKS[LEFT(I)]-1;     { PHILOSOPHER FORK COUNT   }
 END;{ PICKUP }
```

Fig 7—A possible solution to indefinite postponement *blocks a philosopher from Pickup until that philosopher has waited the longest to eat.*

philosopher's neighbors. If the waiting philosopher gets bypassed a set number of times, the program blocks the neighbors until the waiting philosopher has a chance to eat. This solution allows greater, but not maximum, parallelism. **EDN**

Author's biography



Peter H Mackie is president of Interactive Technology, Portland, OR. Before founding that firm, he spent 17 yrs at Tektronix Inc, where he managed a variety of corporate efforts in testing and measurement. Peter holds a degree in electrical engineering.

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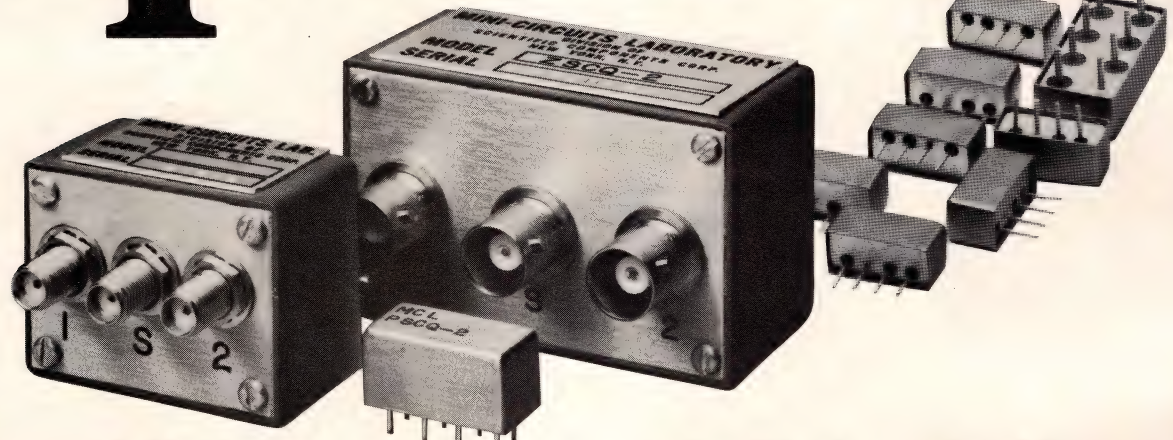

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		Typ.	Min.	Typ.	Max.	Max.	Max.	Each	Qty.
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PSCQ-2-3.4	3.0-3.8	30	25	0.4	0.7	3.0	1.2	16.95	(5-49)
PSCQ-2-6.4	5.8-7.0	30	25	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-7.5	7.0-8.0	35	25	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-10.5	9.0-11.0	25	20	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-13	12-14	29	25	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-14	12-16	30	25	0.3	0.6	3.0	1.8	16.95	(5-49)
PSCQ-2-21.4	20-23	30	25	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-50	25-50	30	20	0.3	0.7	3.0	1.5	19.95	(5-49)
PSCQ-2-70	40-70	25	20	0.3	0.7	3.0	1.2	19.95	(5-49)
PSCQ-2-90	55-90	30	20	0.3	0.7	3.0	1.2	19.95	(5-49)
PSCQ-2-120	80-120	25	18	0.3	0.7	3.0	1.5	19.95	(5-49)
PSCQ-2-180	120-180	23	15	0.3	0.7	4.0	1.2	19.95	(5-49)
PSCQ-2-250	150-250	23	18	0.4	0.8	4.0	1.5	19.95	(5-49)
PSCQ-2-400	250-400	22	16	0.4	0.9	4.0	1.5	19.95	(5-49)
PSCQ-2-450	350-450	22	16	0.4	0.9	4.0	1.5	19.95	(5-49)
ZSCQ-2-50	25-50	30	20	0.3	0.7	3.0	1.5	39.95	(4-24)
ZSCQ-2-90	55-90	30	20	0.3	0.7	3.0	1.2	39.95	(4-24)
ZSCQ-2-180	120-180	23	15	0.3	0.7	4.0	1.2	39.95	(4-24)
ZMSCQ-2-50	25-50	30	20	0.3	0.7	3.0	1.5	49.95	(4-24)
ZMSCQ-2-90	55-90	30	20	0.3	0.7	3.0	1.2	49.95	(4-24)
ZMSCQ-2-180	120-180	23	15	0.3	0.7	4.0	1.2	49.95	(4-24)

*Average of coupled outputs less 3 dB   Impedance 50 ohms all models

62 Rev. O

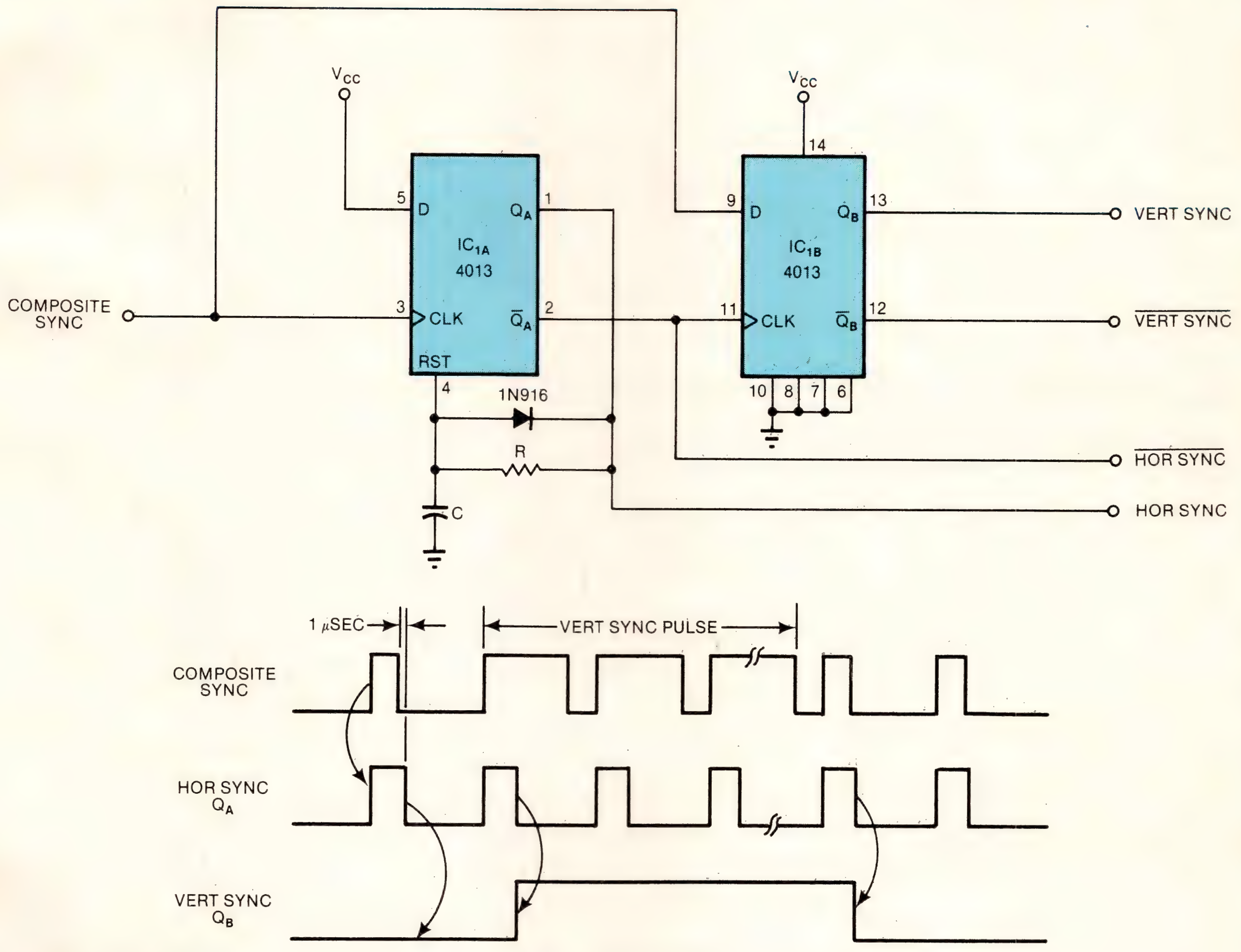
Sync separator uses only one IC

Jack Gershfeld
Conrac Corp, Covina, CA

You can separate horizontal and vertical sync signals with a simpler circuit than one described in an earlier Design Idea (EDN, May 26, pg 204); this circuit (**figure**) uses one 4013 dual flip flop and four passive components. IC_{1A} serves as a one-shot whose output pulse is slightly longer than the width of a horizontal sync pulse. Initially, it's reset and ready for triggering. When it's triggered with a horizontal sync, Q goes HIGH and capacitor C starts to charge through R. When the voltage across C is sufficiently high, IC_{1A} gets cleared and its Q output goes LOW, forward-biasing the diode and discharging C.

IC_{1A} is then ready for triggering again. At this time, $\overline{Q}$ goes HIGH and data gets clocked into IC_{1B}. For horizontal pulses, this clock is always LOW, but during vertical sync, the D input of IC_{1B} is HIGH. Therefore, after the clock, the Q output of IC_{1B} goes HIGH. The first subsequent horizontal sync then resets IC_{1B}, and its Q output goes LOW again. Choose R and C so that the output pulse is about 1 μsec longer than the horizontal-sync width. **EDN**

To Vote For This Design, Circle No 453



A dual D flip flop *separates vertical and horizontal sync pulses.*

Transistor clipper provides flat-top output

Rudy Stefenel
San Jose, CA

If you use the diode clipper shown in **Fig 1a** to clip a sine wave, you won't get a perfect flat-topped waveform because of the diode's forward characteristic. A simple transistor circuit (**Fig 1b**) does a much better job, however, because the transistor's base gets its signals from the circuit input and output.

You can understand the transistor circuit's operation by looking at the effect of each base signal separately. **Fig 2a** shows the circuit with the base signal coming only from the output—a configuration that provides the same result as **Fig 1a**'s diode clipper. **Fig 2b,** on the other hand, shows the circuit with the base signal coming only from the input. With this configuration, the output actually sags, because as the transistor's base gets driven harder as a result of the input pulse's rounded top, the collector saturates harder.

The combination of the two base signals thus provides the flat-top characteristic. For different transistor types, the optimum resistor values might vary.

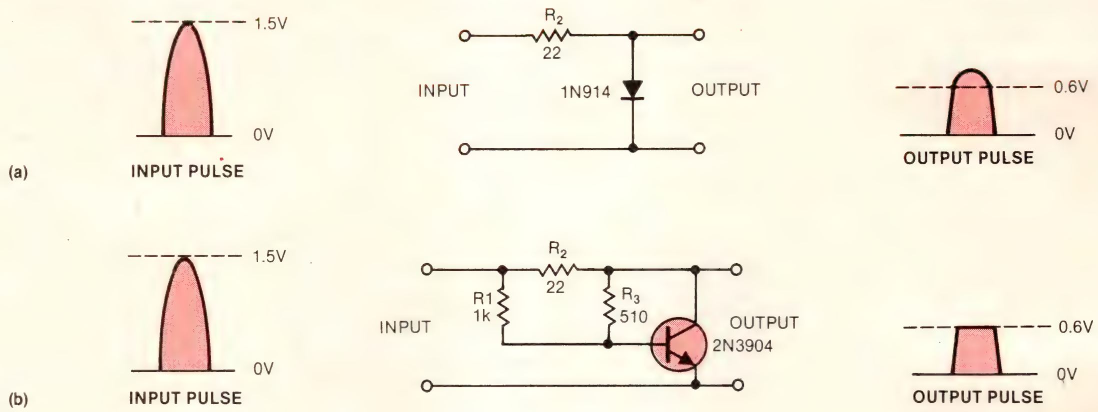


Fig 1—A simple diode clipper (a) *provides a signal with a rounded top when driven by a sine wave. Substituting a transistor whose base accepts two input signals* **(b)** *results in a flat-top characteristic.*

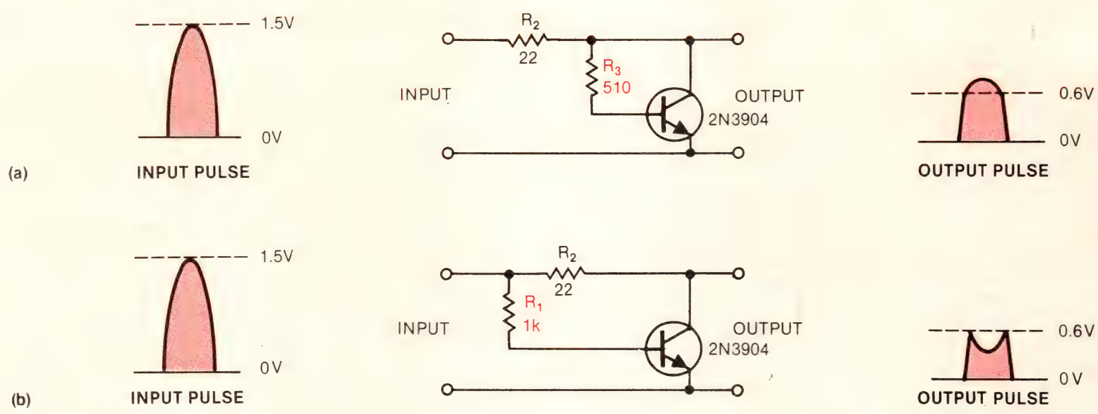


Fig 2—Without the resistor *from the input to the transistor base* **(a), Fig 1b***'s circuit's action is the same as that of* **Fig 1a***'s diode clipper. And with the resistor from the output to the base removed* **(b),** *a sag appears in the pulse's center because the transistor is driven harder there.*

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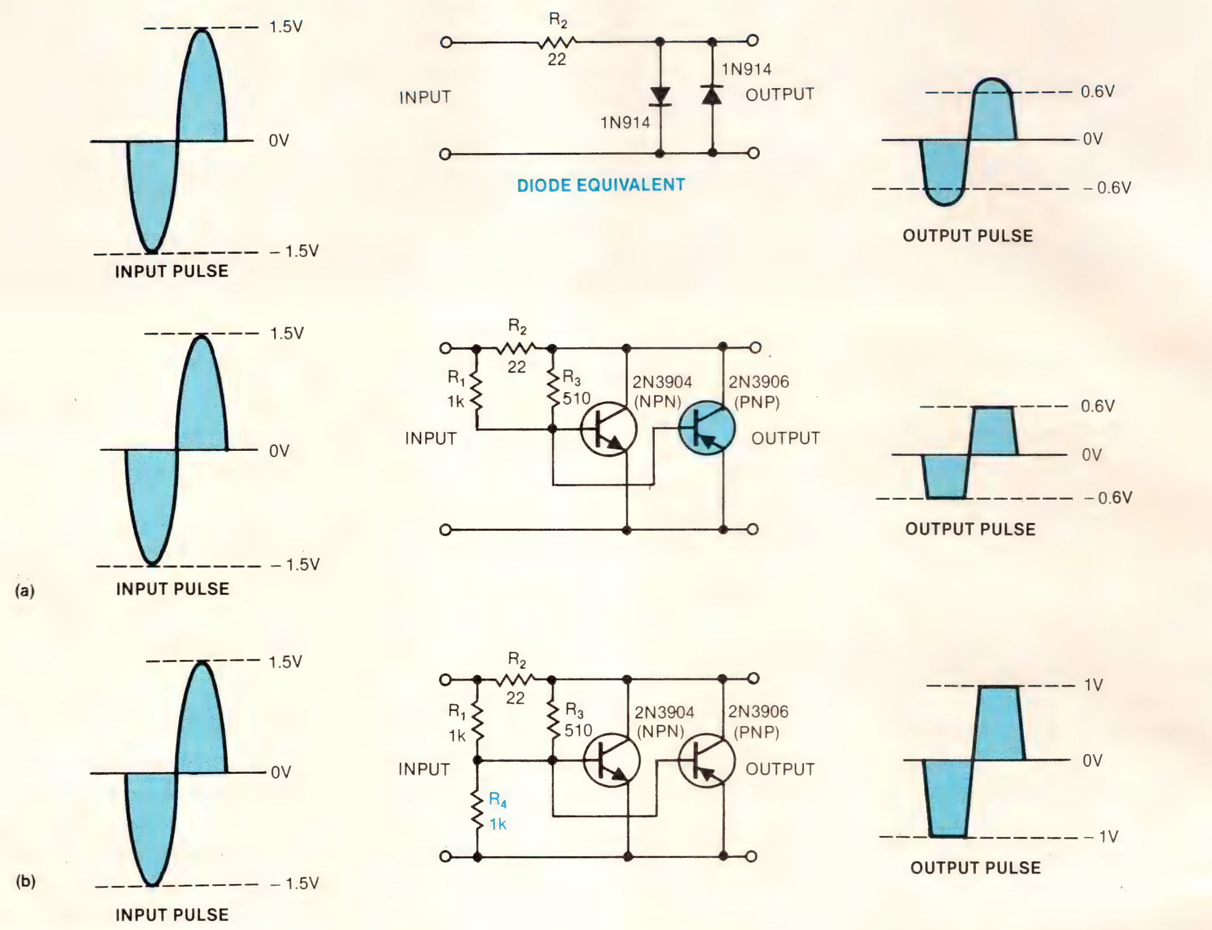


Fig 3—Symmetrical action *results when you add a complementary transistor to* **Fig 1b***'s design* **(a)***. And adding a resistor* **(b)** *raises the complementary circuit's clipping level.*

Add one component—another transistor—to **Fig 1b**'s circuit, and you have a symmetrical clipper, shown in **Fig 3a** along with its diode counterpart. And add another resistor, and you can raise the clipping-voltage level (**Fig 3b**). This latter circuit functions at levels into the tens of volts. However, at higher voltage levels, it's more efficient to use zener diodes. **EDN**

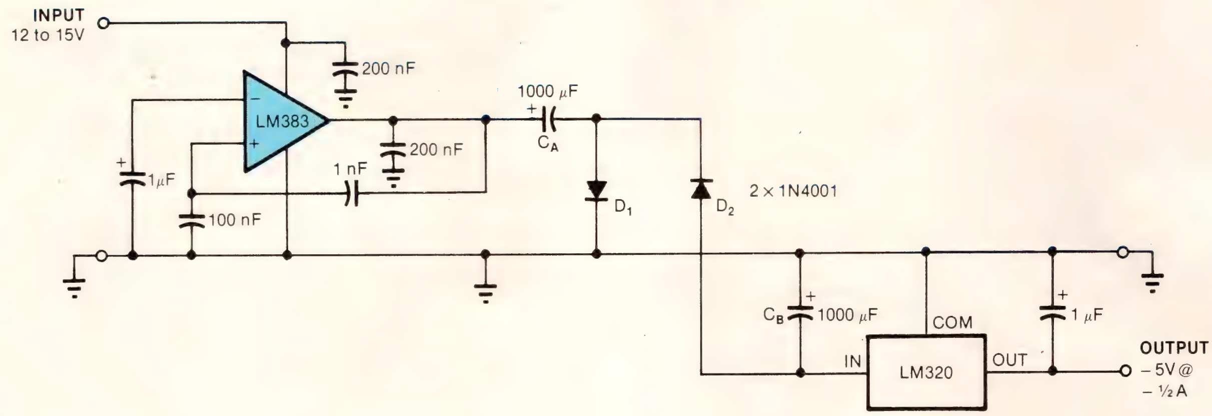
To Vote For This Design, Circle No 454

Use a power amp to convert 12V to −5V

Mitchell Lee
National Semiconductor Corp, Santa Clara, CA

Frequently you need a negative supply to power logic or memory chips but have only positive voltages available—in battery-operated systems, automotive systems and remote devices fed by a cable or bus with one supply voltage, for example. The circuit shown in the **figure** provides such a negative voltage, delivering ½A at −5V from an input of 12 to 15V.

The LM383 power amplifier forms a 1-kHz square-wave oscillator capable of driving 3.5A pk into the pumping capacitor, C_A. On positive half cycles, the



An LM383 power amplifier *acts as a square-wave-oscillator charge pump, converting a 12V input into −5V at ½A.*

amplifier's output charges C_A through D_1; D_2 is reverse biased and does not conduct. On negative half cycles, however, the LM383's output holds C_A's positive terminal at near-ground potential, forcing the negative terminal to dump charge into C_B through D_2. The LM320 regulates the voltage across C_B to −5V. Note that this circuit does not require any inductors or resistors. **EDN**

To Vote For This Design, Circle No 455


Gates
Energy Products
2 VOLT

Put a 16-bit output port on an 8-bit μP

Sheila Thornton
ADT Security Systems, New York, NY

You can build 12- to 16-bit output ports for an 8-bit μP using less hardware than required in the design proposed in "Interface 12- and 16-bit DACs to an 8-bit μC" (EDN, November 25, 1981, pg 163). And the design presented here employs the straightforward technique of address latching to achieve a higher throughput rate.

In the read/write timing diagram for the Z80 μP (**Fig 1**), you can see that if Data Stable time A is long enough to enable use of the negative $\overline{WR}$ transition for latching output data, you can latch the address outputs as well. (Time A is at least 30 msec, even for a Z80A running at 4 MHz.) You can thus use eight data lines and eight address lines to write any number to 64k to a peripheral in one write operation; you only need have available a block of 256 adjacent addresses. Moreover, if the block used is occupied by ROM, you needn't sacrifice memory space or supply additional address-decoding circuitry.

Fig 2 shows a 4-chip implementation of this approach for a Z80-based μC. Gates U_{1A} and U_{1B} keep the ROM disabled during writes to the ROM address, and gate U_{1C} supplies a positive clock pulse whose leading edge latches U_2, U_3 and U_4. **Fig 3** contains the Z80 code that exploits this hardware to write the sequence 0 through 4095 to the output

Continued on pg 164

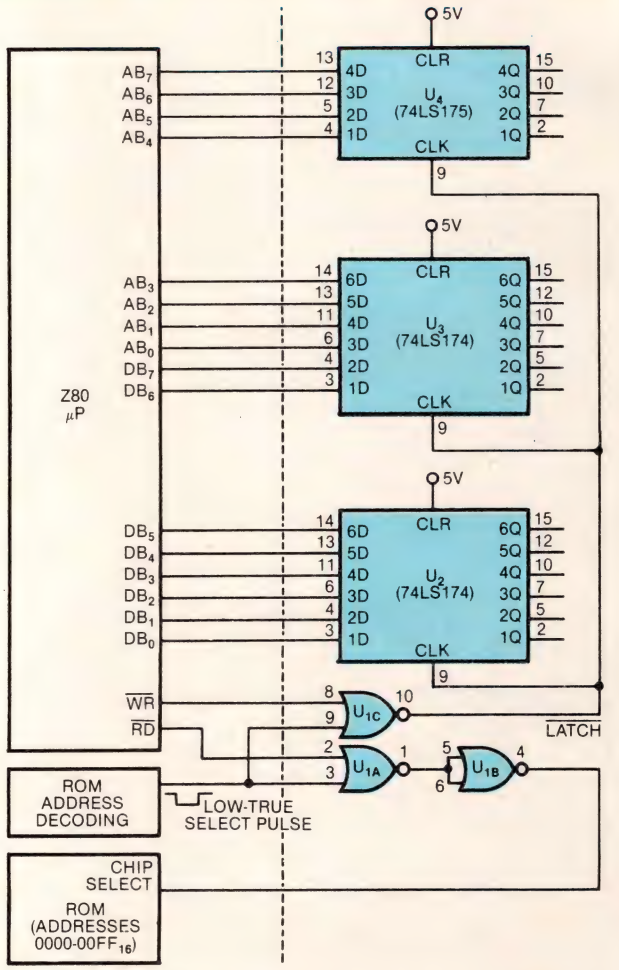


Fig 2—You can implement a 16-bit port for an 8-bit Z80 μP *with only four additional ICs.*

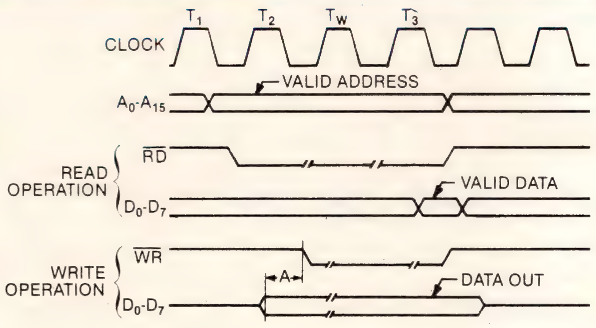
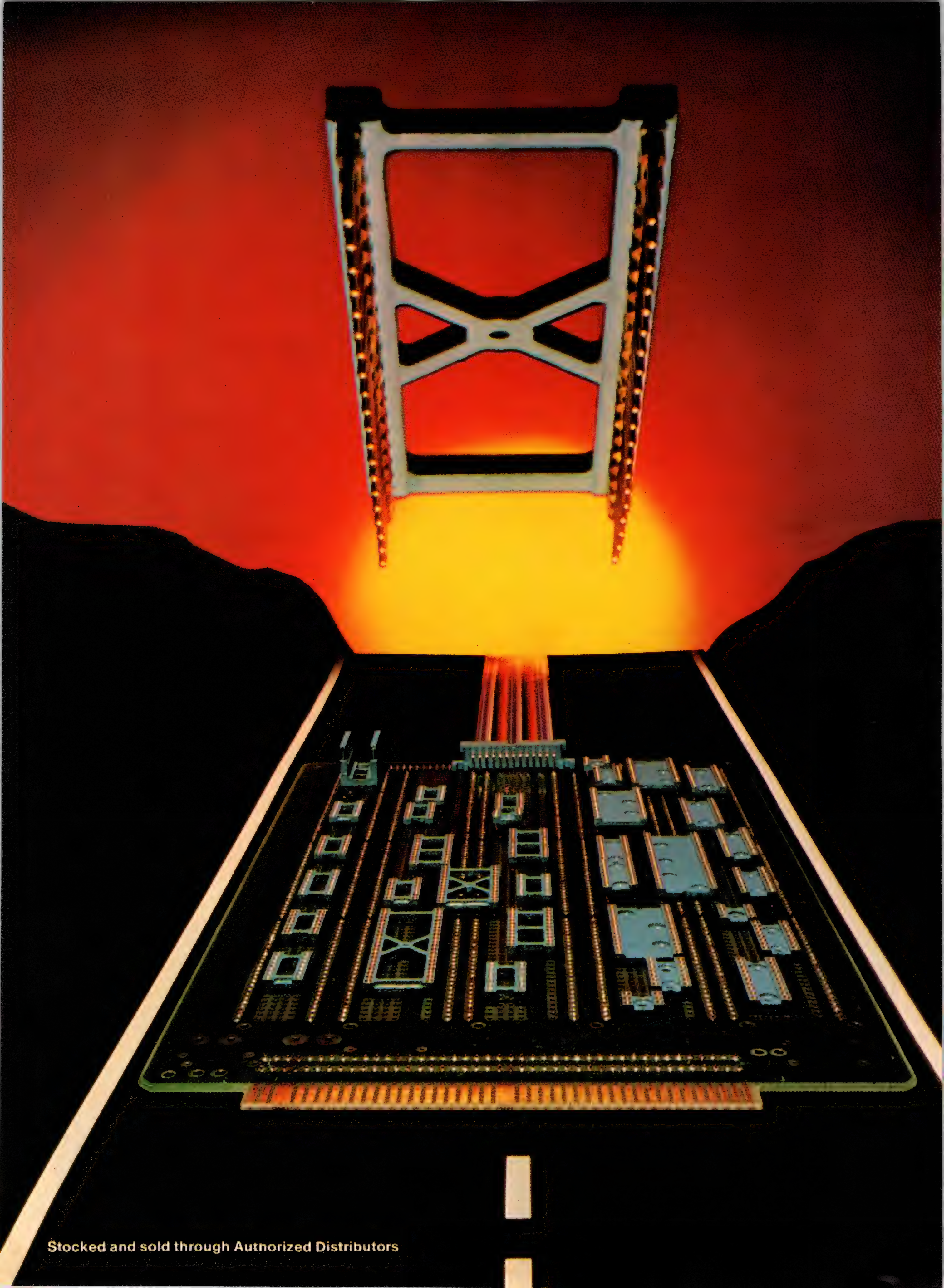


Fig 1—A data-stable time long enough *to permit use of a negative $\overline{WR}$ transition for output-data latching allows you to latch address outputs as well.*

ADDR	CODE	LABEL	INSTRUCTION	COMMENTS
4400	3E 00		LD A, 0	CLEAR A AND HL TO SERVE AS DATA
4402	21 00 00		LD HL, 0	AND ADDRESS REGISTERS FOR PORT
4405	77	WRITE	LD (HL), A	WRITE A TO ROM BASE ADDRESS + L
4406	3C		INC A	A + 1 → A
4407	20 FC		JR NZ, WRITE	IF A ≠ 0, JUMP RELATIVE TO WRITE
4409	2C		INC L	L + 1 → L
440A	CB 65		BIT 4, L	NOT LA → Z
440C	28 F7		JR Z, WRITE	IF LATCH, JUMP RELATIVE TO WRITE
440E	C9		RET	RETURN

Fig 3—Capable of executing in 47.3 msec *with a 2-MHz clock, this Z80 code writes numbers 0 through 4095 to an output port.*



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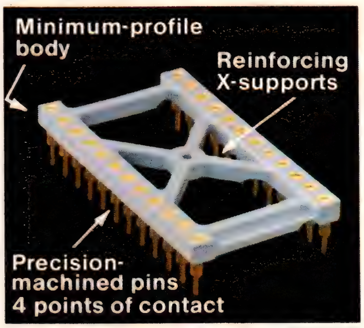

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CIRCLE NO 61

port. This code executes in 47.3 msec with a 2-MHz clock or 31.5 msec at 3 MHz (possible on a Z80A). With similar programming, you can use the latched address for tasks such as selecting an output channel from a DAC.

With minor modifications, you can apply this technique to virtually any μP. For use with the 650X, for example, the circuit must provide a latching signal because the Write transition on the R/W line occurs before the address and data outputs are established **(Fig 4).**

By combining R/W with ϕ_2 and adding capacitor C_D **(Fig 5),** you can delay the time at which $\overline{\text{LATCH}}$ reaches the flip flops' triggering voltage to about 0.25 μsec past timing reference B. This method tolerates variations both in C_D and the data-setup

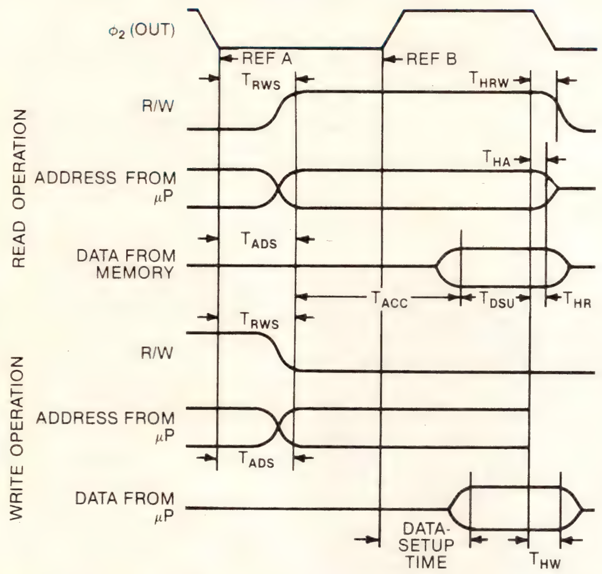

Fig 4—Modifying Fig 2's circuit *to suit 650X-μP timing requires generation of a latching signal.*

ADDR	CODE	LABEL	INSTRUCTION	COMMENTS
0200	D8		CLD	SET HEX MODE
0201	A9 00		LDA #0	CLEAR A AND X TO SERVE AS DATA
0203	A2 00		LDX #0	AND ADDRESS REGISTERS FOR PORT
0205	18	CLEAR	CLC	0→C
0206	9D 00 0F	WRITE	STA PORT, X	WRITE A TO PROM BASE ADDRESS + X
0209	69 01		ADC #1	A+1→A
020B	D0 F9		BNE WRITE	IF A≠0, BRANCH TO WRITE
020D	E8		INX	X+1→X
020E	E0 10		CPX #10H	CHECK IF X = 16D
0210	D0 F3		BNE CLEAR	IF NOT, BRANCH TO CLEAR
0212	60		RTS	RETURN

Fig 6—Executing in 41.1 msec *with a 1-MHz clock, this code runs on a 650X-μP-based system, replacing* ***Fig 3****'s Z80 code.*

time (typically 150 nsec at 1 MHz). The rest of the design is similar to that for the Z80, using only a few gates in addition to the latches. The 650X code **(Fig 6)** performs the same function as the **Fig 3**'s Z80 code. Execution time equals 41.1 msec at 1 MHz.

EDN

NEXT TIME

EDN's October 13 issue will feature a Special Report on capacitors. Also look for design features on

- How to deal with capacitor dielectric absorption (soakage)
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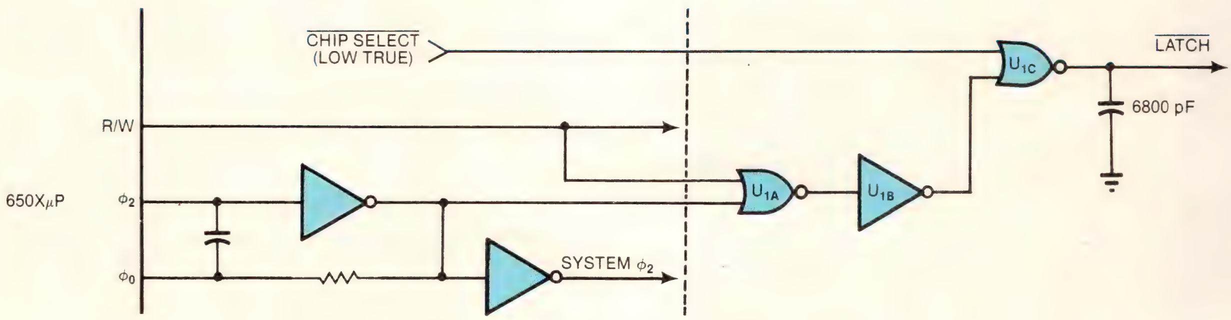

Fig 5—Combining the R/W and ϕ_2 signals *of a 650X μP and employing capacitor C_D meets* ***Fig 4****'s timing requirements.*

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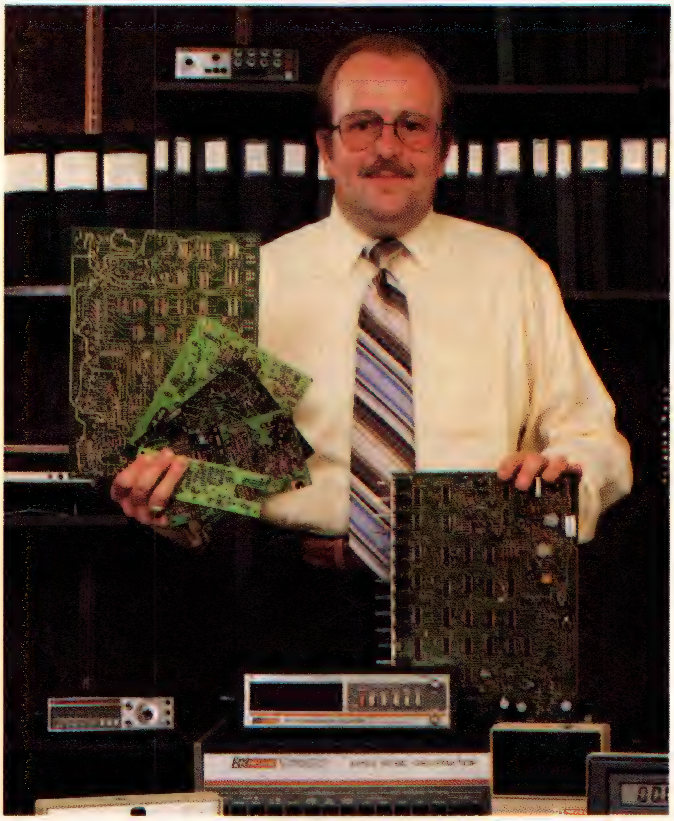

J. W. Jaroszewski, Plant Manager, Dynascan Corporation

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CIRCLE NO 62

Add I/O-port commands to 8085 monitors

Frank Engelman
GE Medical Systems, Rancho Cordova, CA

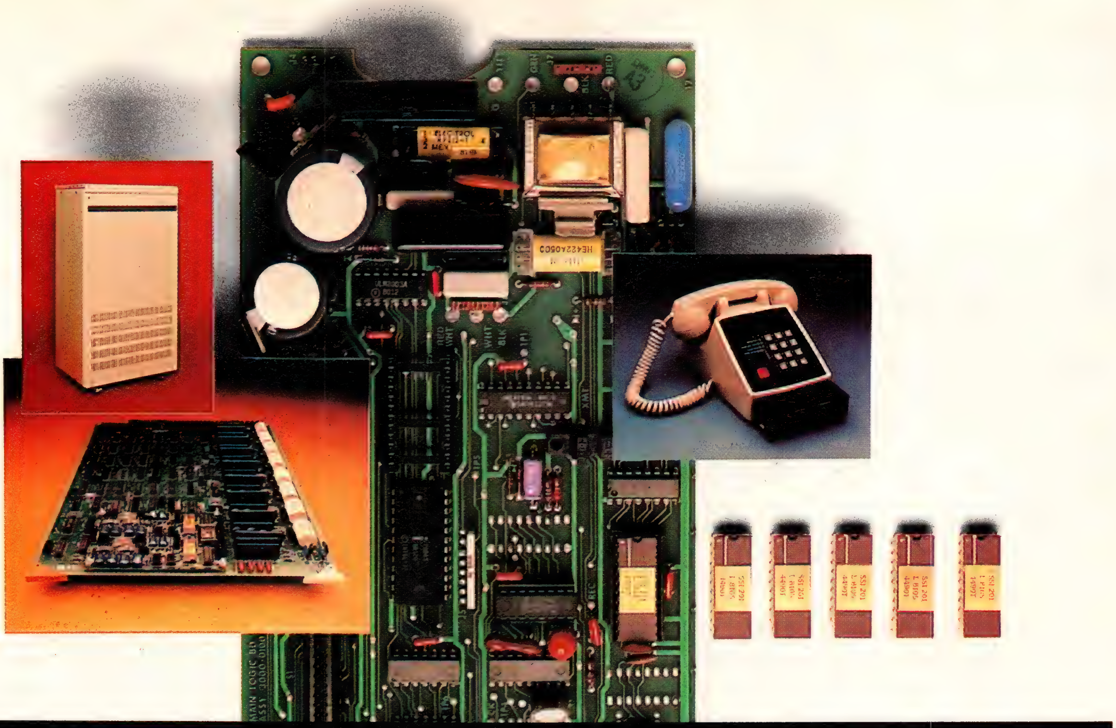
If you've ever written a PROM-based monitor routine for an 8080- or 8085-based system that includes I/O-mapped ports, you've undoubtedly encountered difficulty providing user selection of those ports. The problem arises because these μPs require that the port number be coded in the memory byte immediately following the IN or OUT instruction. With PROM, this requirement prevents changing the port number.

One way to solve this problem is to use the "not recommended" technique of self-modifying code. Basically, you provide room in RAM for a modifiable subroutine that you call from your main program in PROM. The main program constructs the RAM routine by writing an IN or OUT instruction, the port number and a RETURN (**figure**). An even simpler approach leaves the instructions in place and changes only the port number. **EDN**

```
LXI    H,INPORT    ;POINT AT RAM       INPORT: 0DBH
MVI    M,0DBH      ;WRITE "IN" INST            (port#)
INX    H           ;NEXT LOCATION              0C9H
MOV    M,A         ;WRITE PORT #
INX    H
MVI    M,0C9H      ;WRITE "RET" INS
CALL   INPORT      ;EXECUTE INPUT

       PROM-RESIDENT                   RAM-RESIDENT
       CODE                            CODE
```

Self-modifying code *permits user selection of I/O ports for 8080 or 8085 μPs.*



PCB's and photos of PBX and transaction terminal courtesy of American Telecom, Inc. and DMC Systems, Inc.

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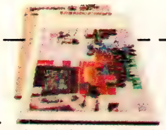

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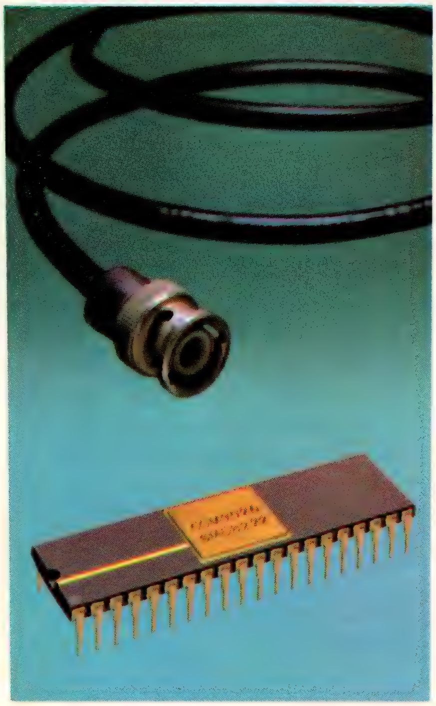

Other functions include address decode, CRC checking and generation and packet acknowledgement and support of up to four 508 byte buffers.

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For information on the COM 9026, contact Standard Microsystems Corporation, 35 Marcus Boulevard, Hauppauge, NY 11788. (516) 273-3100.

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CRT, MAGNETIC AND DATA COMMUNICATIONS CONTROLLER CIRCUITS.

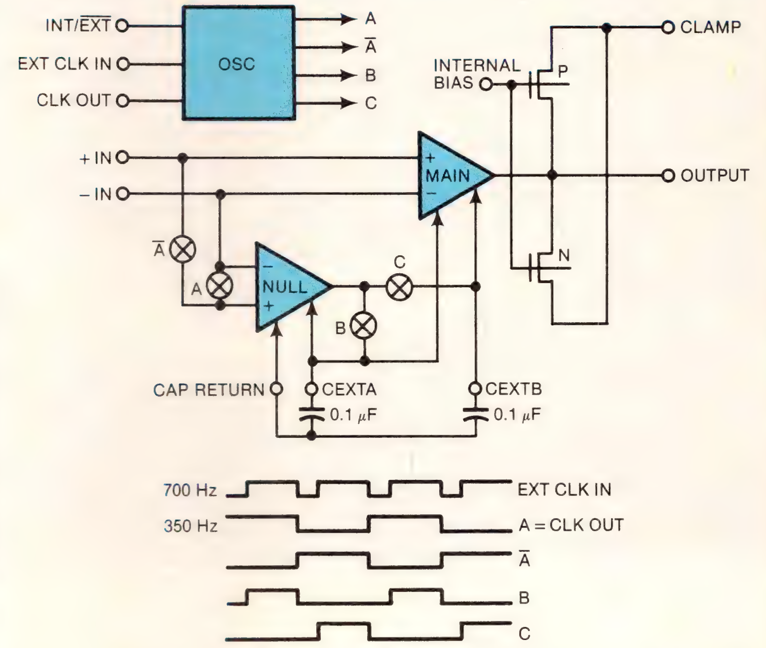
CIRCLE NO 64

Feature Products

CMOS chopper-stabilized op amp also provides low noise specs

Thanks to a redesigned FET input stage and other design modifications, the ICL7652 monolithic precision CMOS op amp achieves an input noise voltage of only 700 nV p-p typ from 0 to 10 Hz and just 200 nV p-p from 0 to 1 Hz.

Brother to its manufacturer's ICL7650 (EDN, April 15, 1981, pg 50), the 7652 sacrifices some of the former device's slew rate (decreased from 2.5 to 0.5V/µsec) and bandwidth (from 2 MHz to 450 kHz) but gains a larger common-mode voltage range: −4.3 to +3.5V. The manufacturer notes that in applications for which it's intended, such as thermocouples, strain gauges and pH meters, dc performance is the main criterion. And in that area, the 7652 matches its relative.



Bringing low-noise performance to high-precision devices, *the ICL7652 CMOS chopper-stabilized op amp features a 700-nV p-p input noise voltage from 0 to 10 Hz (200 nV p-p from 0 to 1 Hz). Precision is maintained via a ±0.7-µV offset voltage with a temperature drift of 0.01 µV/°C and long-term drift of 100 nV/√month.*

High precision

Typical input specs include ±0.7-µV offset voltage at 25°C (±1 µV over temperature). Offset drift with temperature measures 0.01 µV/°C, and drift with time equals 100 nV/√month. The device's larger FET inputs raise the input-bias-current spec to 25 pA with a 5-pA offset current.

Internally compensated for unity gain, the 7652 features gain, CMRR and PSRR of more than 120 dB, ±4.7V min output-voltage swing and a 4.5 to 16V supply-voltage range. With nominal ±5V supplies, it consumes just 35 mW.

The op amp incorporates a main and a nulling amplifier, an on-board clock oscillator, overload-recovery clamp circuit and intermodulation - compensation network. The main amplifier always connects from input to output, while the nulling amplifier, under control of the chopping-frequency oscillator, alternately nulls itself and the main amplifier.

Careful balancing of the input switches minimizes chopper-frequency charge injection at the input terminals and feedforward-type injection into the compensation capacitor—the main cause of output spikes in this type of circuit.

Intermodulation effects are substantially reduced by feeding the nulling circuit a dynamic current that cancels that portion of the input signal deriving from finite ac gain. This action keeps the open-loop phase shift to less than 10° at chopper frequency.

The device's output-clamp pin reduces overload-recovery time by cutting the gain just before maximum output.

The ICL7652 comes in 8- and 14-pin plastic DIPs, an 8-pin TO-99 and a 14-pin Cerdip. Available temperature ranges include 0 to 70, −20 to +85 and −55 to +125°C. $4.50 (100) in plastic.

Intersil Inc, 10710 N Tantau Ave, Cupertino, CA 95014. Phone (408) 996-5000.

Circle No 456

Do your designs reflect the latest thinking in IC usage?

Be sure.

Attend a new series of conferences for IC users:

PRACTICAL DESIGN WITH INTEGRATED CIRCUITS

Northern California (Sunnyvale Sheraton)
Nov. 15-16, 1982. Linear Integrated Circuits
Nov. 17-19, 1982. Gate Arrays/Custom/Semi-Custom

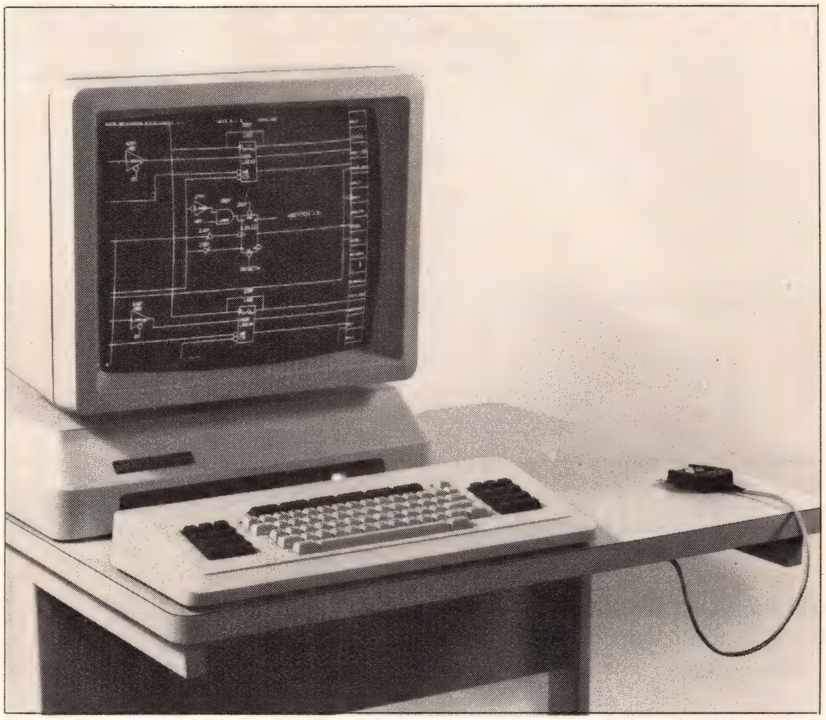
Not every engineer needs to be aware of the latest semiconductor devices (microprocessors, linear ICs, semi-custom chips, LSI). But if you're one of the engineers responsible for new equipment or system design at your company, these conferences could be very important to you. Every talk in the program is presented by an IC manufacturer; each talk concerns a new IC and ways to use it to improve existing designs.

System designs often have short lifetimes. For your next design to reflect the latest concepts in applying integrated circuits, plan to attend each program in this conference series. Individual conferences on gate arrays/custom/semi-custom ICs, microprocessor/digital devices, and linear ICs will comprise the series of programs known as "PRACTICAL DESIGN WITH INTEGRATED CIRCUITS."

Each attendee receives a comprehensive proceedings, the latest handbooks, application notes, manuals and other technical literature. All conference talks are new and previously unpublished.

Multiuser logic-design system supports structured project development

A 4-station computer-aided hardware-design tool, the SCALD (structured computer-aided logic design) system supports schematic-entry and documentation tasks and controls interactive simulation and timing-verification routines. Its workstation-based graphics editor, component libraries, workstation- or host - based design compiler and schematic post-processor let you develop complex circuits hierarchically, beginning with fundamental function definitions and expanding each major circuit block one level at a time until you've described the design in terms of actual circuit elements.



Embodying a hierarchical design philosophy, *the SCALD system lets you develop logic circuits in a top-down manner. One SCALD processor supports as many as four graphics workstations; optional software performs design compilation and analysis.*

A 68000-μP-based cluster controller that runs under Bell Labs's UNIX forms the SCALD system's heart. The processor includes 1M bytes of error-correcting RAM, a 33M-byte Winchester disk drive and a ½-in., 1600-bpi streaming tape drive. Standard RAM supports one remote workstation; each additional terminal requires a 512k-byte RAM expansion.

Available communication interfaces include 800-bps VAX-11 and 56k-baud IBM 370 ports for running host-based software, as well as VT-100 and IBM 3277 emulators for electronic mail and custom software.

Each SCALD workstation features an 8086 central processor, a 20-in., 4-intensity-level raster display, a detachable keyboard and a data tablet. Workstations connect to the cluster controller through a high-speed serial link and can operate 500 ft from the CPU.

To verify circuit operation during all design-cycle phases, optional SCALD software supports timing analysis and functional simulation. The timing verifier checks for switching problems such as race conditions, setup and hold violations, glitches and pulse-width errors, isolating potential faults at early design stages. It performs an absolute - value - independent analysis, observing system operation over a range of rise and fall times, propagation delays and output conditions.

To ensure that final designs don't need tight component tolerances, the verification routine checks circuit activity using a variety of permutations resulting from combinations of minimum and maximum specs.

To complement the timing analyzer, the SCALD logic simulator provides high-speed interactive analyses of circuit operation on a cycle-by-cycle basis. Because the simulator assumes proper logic timing and observes circuit activity in a series-parallel manner, you can debug complex systems without consuming excessive amounts of processor time. Fast analysis allows you to debug microcoded firmware or software as well as simple combinatorial circuits.

To simplify schematic entry, SCALD component libraries contain graphical, simulation and physical data for standard TTL, STTL, LSTTL, 10K and 100K ECL and MOS memories. In addition, you can combine multiple devices to form a graphical representation of wide parallel buffers and bus compo-

nents as single blocks. A post-processor routine converts the SCALD graphical database into a user-definable output format for use with remote physical CAD systems or other automated design tools.

Entry-level system, $67,500 including cluster controller, one workstation, UNIX operating system and graphics editor; typical 4-station system, $138,000; device-library software, $7500 per component family. Optional analysis tools: SCALD compiler, $7500; post-processor, $15,000; timing verifier and simulator, $45,000 each. Communications interfaces, $2200 to $3750.

Valid Logic Systems Inc, 650 N Mary Ave, Sunnyvale, CA 94086. Phone (408) 773-1300.

Circle No 457

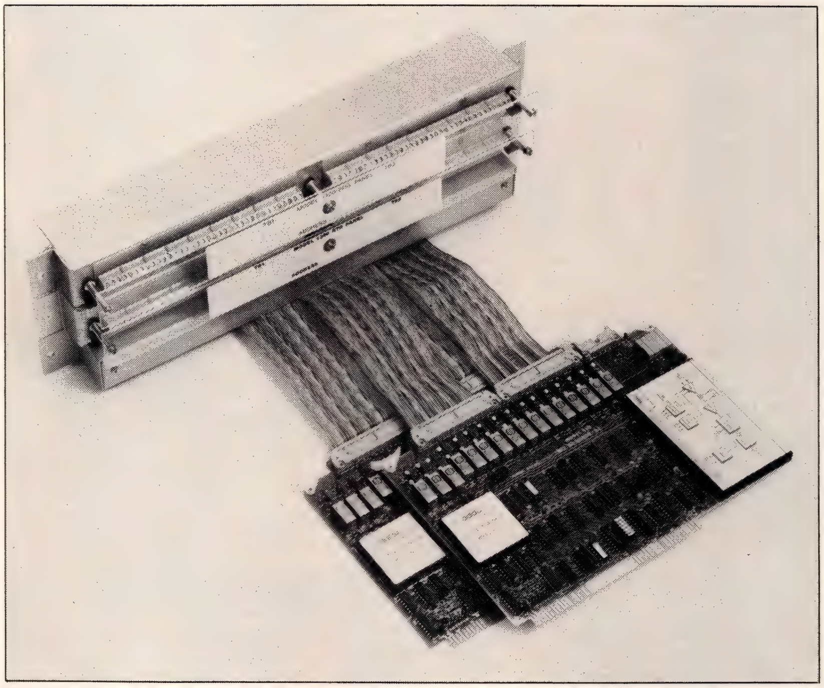
8- or 16-channel screw-terminal panels condition analog signals for system buses

With their associated multiplexer-A/D-converter boards, the 1300/RTD and 1300/BDG screw-terminal panels interface low-level analog signals to LSI-11 and TM990 computer buses and to the Multibus. Both panels contain active components that provide input signal conditioning between their clamp-type screw terminals and mating-board cables.

Requiring an external ±15V supply for operation, the 1300/RTD panel interfaces and powers 100Ω 3-wire platinum resistance temperature detectors (RTDs) used in data-acquisition systems. It acts as the RTD's bridge-completion, linearization and excitation unit. Four screw terminals secure the RTD's three active wires and shielded common ground.

The 1300/RTD senses the RTD's resistance change over temperature with the RTD connected as the external arm of a 4-arm bridge circuit. A built-in 10V reference source serves as the bridge excitation supply, and an adjustable amplifier compensates for bridge and RTD nonlinearity. Two other trimmers control the bridge's offset and reference voltages.

Handling eight or 16 RTDs (channels), the 1300/RTD provides 200-mV nominal full-scale outputs over 200°C. Connected via a 6-ft, 50-conductor shielded flat ribbon cable, these outputs get multiplexed and digitized by the 1112 or 1113 Series boards for the LSI-11 bus, 710 Series boards for the Multibus and 410 boards for the TM990 bus.



Featuring eight or 16 input channels, *the 1300/RTD and 1300/BDG screw-terminal panels process low-level analog signals (from RTDs and strain gauges, respectively) for delivery to the Multibus or the TM990 or LSI-11 computer bus via flat cable and an integral multiplexer-A/D-converter board.*

Similar to the 1300/RTD, the 1300/BDG panel serves as a bridge-completion and linearization unit for 350Ω strain gauges and load cells. Key differences from the RTD panel include direct bridge excitation from the 10V reference, 350Ω bridge resistors and 30-mV FS outputs.

Both 19×1.75-in. panels come in single or dual widths with one or two 8-channel terminal blocks. 1300/RTD, $595; 1300/BDG, $540.

ADAC Corp, 70 Tower Office Park, Woburn, MA 01801. Phone (617) 935-6668.

Circle No 458

Data-acquisition/control instrument features HP-IL compatibility

Within its mainframe, the battery - powered Model HP3421A includes a scanner, an A/D converter, a frequency counter, a display and HP-IL interface circuitry that allows you to control it with any HP-IL-compatible device (eg, HP-41CV handheld calculator, HP-85 desktop computer). And an IEEE-488 option lets you use a more sophisticated computer for control.

The 3421A scans 30 channels (denoting closures via a front-panel LCD) and measures ac and dc voltage, 2- and 4-wire resistance, frequency, and temperature. Thermocouple compensation is built in, and Power Down mode, enabled by an HP-41C controller command, can extend battery life from 10 hrs to more than a month.

The internal A/D converter achieves 1-μV sensitivity. Although basic converter resolution equals 5½ digits, you can program 4½- or 3½-digit operation to increase reading rate.

A low-cost data-acquisition and control system *results when you control the HP-IL-compatible Model HP3421A with the HP-41CV handheld calculator.*

The ADC requires no adjustments: All calibration constants are stored in a CMOS RAM and protected by a 10-yr lithium battery.

You can add optional features by installing plug-in cards. Option 020, for example, is a 10-channel multiplexer; you can configure two of its channels as actuators with a 2A/250V ac switching capability. The mainframe accommodates three such cards.

In addition, you can use Option 040, a breadboard card, to add signal conditioning or gain access to the mainframe's backplane. And Option 050, a digital-I/O card, furnishes eight individually isolated bits of input or output. A digital-trigger command operates through this I/O board; when the 3421A senses the correct trigger word, it performs a complete scan and provides a record of the input conditions at the time the trigger occurred, all without controller intervention.

When you use the -41CV calculator for control, a special ROM and overlay panel for the calculator extend the 3421A's versatility by adding functions such as thermistor and RTD linearization. The 3421A includes linearization capability for Type T thermocouples, but other types (J, K, E, R and S) need the linearization routine in the -41CV control ROM. $1300 for basic mainframe.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 459

Color-graphics system works in three dimensions

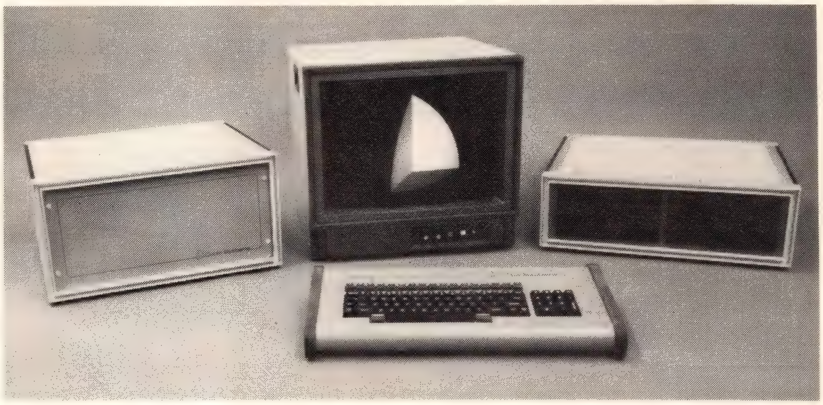
Building on the processing power of the 16-bit 8086 μP and its 8087 numeric coprocessor, the CS-3 system uses proprietary imaging firmware to create and manipulate 2- and 3-dimensional vector drawings. Built-in routines provide graphics functions that you can call up from FORTRAN, BASIC, PASCAL, C and 8086-assembler applications programs.

Once the outlines are drawn, you can select such object properties as coloring, smooth shading, antialiasing (to straighten diagonal lines) and hidden-line and -surface removal. You can choose any combination of 4096 colors from a palette of 16 million.

Further, you can rotate, scale or reposition the image for proper orientation and even change the viewpoint and light source. And when you discover which object drawings you are using repeatedly, you can create image data macros that build an image for you.

The system comes with a 95-key detachable keyboard; input-device options include a data tablet, light pen and joystick. To integrate the CS-3 with other imaging systems,

Feature Products



Featuring 3-dimensional imaging capability, *the CS-3 system can function as an intelligent color-graphics terminal for time sharing and distributed processing.*

you can choose an optional Ethernet interface and a software preprocessor that lets the CS-3 emulate other terminals such as the Tektronix 4014.

The CPU and memory come in a 12-slot Multibus card cage—seven slots accommodate optional equipment. The system includes 128k bytes of scratchpad, expandable to 512k.

The CS-3 uses a 512×512 color raster-scan display generator with 12-bit/pixel resolution to display images on a 20-in. RGB-type color monitor. The system can store two independent planes of an image, allowing you to modify one plane while viewing the other.

You can configure the system as a highly intelligent color-graphics terminal for time-sharing and distributed-processing applications. Add an optional dual 8-in. floppy-disk subsystem or a memory subsystem that combines an 8-in. floppy and a 10M-byte hard disk and you have a stand-alone computer-graphics system that uses CP/M-86.

In either case, the system provides an RS-232C interface that runs at 19.2k baud and two auxiliary serial ports for tying into other hardware. Stand-alone system, from $9980.

Cubic Systems, 2215 Spaulding Ave, Berkeley, CA 94703. Phone (415) 540-5733.

Circle No 460

NEXT TIME

EDN's October 13 issue will feature a Special Report on capacitors. Also look for design features on

- How to deal with capacitor dielectric absorption (soakage)
- How to choose among the sometimes confusing array of waveform-digitizer products.

Leading off the issue will be a Technology Update on optoelectronic ICs. And you won't want to miss our regular Design Ideas department, either.

EDN: Everything Designers Need

RCA says "A board in the hand is worth two in the bush."

Why wait for National? RCA has over 70 Microboards right now. At a fraction of the price.

Lately, National Semiconductor has been making a lot of noise about their line of CMOS board-level products. But consider these facts:

RCA introduced the first CMOS Microboards in 1979.

Today, we offer more than 70 proven Microboard products including computer boards based on the world's best-selling CMOS microprocessor series, the RCA 1800; development systems priced as low as $699*; and the industry's most versatile industrial chassis line.

National offers only 13 products.

Delivery? Off-the-shelf from RCA distributors.

Furthermore, our Microboards speak your language, whether it's BASIC 1, 2 or 3, Micro Concurrent PASCAL**, PLM-1800 or MACROASSEMBLER.

National Semiconductor System	
Board	Price‡
CIM-802 CPU, 2.0 MHZ Memory, PIO	$546
CIM-201 UART-2 required	716
CIM-411 12 Bit A/D (No 8-Bit Available)	952
CIM-311 Power I/O Interface (requires DIB board)	394
CIM-230 DIB Interface	286
CIM-602 8-Card Chassis	295
CIM-610 Voltage Regulator (only supply available)	952
‡NSC OEM Resale Schedule, June 7, 1982.	$4,141

RCA Microboard System	
Board	Price
CDP18S602 CPU, 2.5 MHZ Memory, PIO, UART	$299
CDP18S641 UART	175
CDP18S658 8-Bit A/D	199
CDP18S662 PIO OPTO 22 Interface	225
MSI804 4-Card Chassis	130
CDP18S023 Microsupply	25
	$1,053

But here's the true acid test. If you want a CMOS microcomputer system with these functions:

• 8-Bit Microprocessor • 2 Serial I/O Lines • 8-Bit A/D • Interface to 24 OPTO 22 Modules • Chassis and Power Supply.

The bottom line is, RCA has the lower system cost.

The RCA system takes up less space (4 boards vs. 6) and is one-fourth the price. Compare your own system and see for yourself.

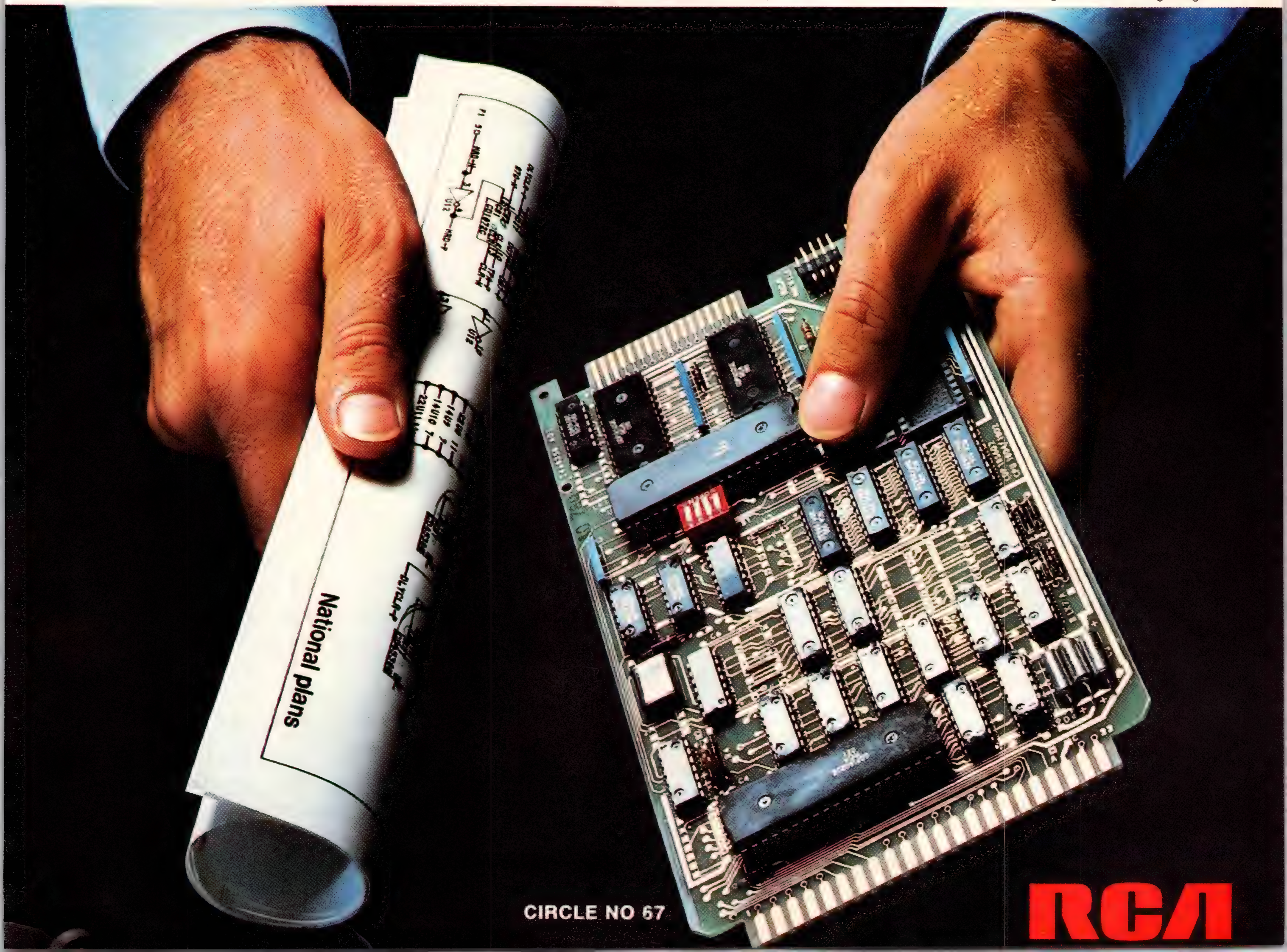
So if you're ready to get on the CMOS bandwagon, talk to the people who invented CMOS and whose Microboards can be found in thousands of systems at work solving real-world problems.

Send for our new comprehensive product line guide and price list.

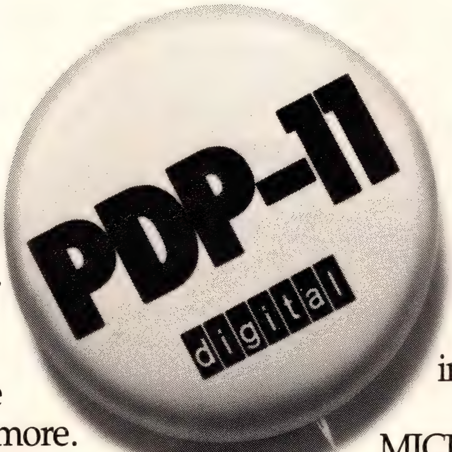
Contact any RCA Solid State sales office, representative or distributor.

Or call (800) 526-3862.

*Optional U.S. distributor resale. Prices are f.o.b. New York. **Tradename of Enertec, Inc. RCA Solid State headquarters: Somerville, NJ. Paris. London. Hamburg. Sao Paulo. Hong Kong.



How to get more



For nearly twenty years Digital has been helping OEMs get more out of computer systems.

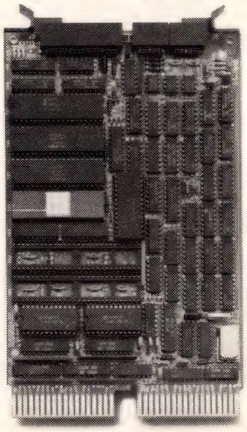
Now we're doing it with micros. And we're doing it the same way we always have. By offering more.

Our 16-bit PDP-11 architecture is the basis for all our microprocessors, single board computers and other LSI-11 micro products. And it is by far the most experienced, most developed, and most complete architecture in micros today.

An investment you can build on.

Since all our micros are compatible, you can reduce your hardware and software development costs considerably. Because you'll never have to start your development from scratch. You can just keep building on your experience with each new product you design.

You can also take advantage of the vast amount of software that's available from third-party vendors, large end-users, and Digital itself.



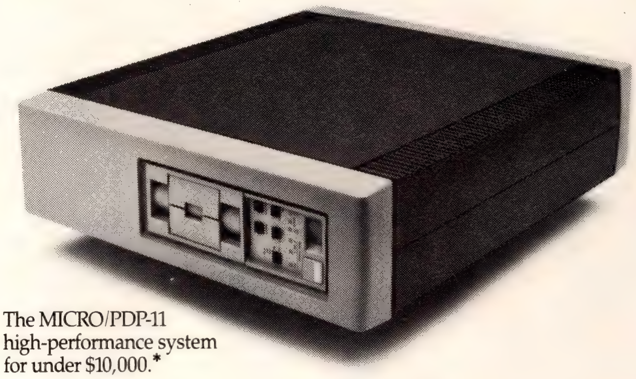
Digital's Falcon: the smallest 16-bit SBC on the market.

In addition, you can work with sophisticated development tools to shorten your time to market. And you won't have to worry about finding programmers, because the PDP-11 architecture is one of the most widely used computer architectures in the world today.

More to choose from.

Digital offers you every level of integration of 16-bit microcomputers.

From our new MICRO/J-11 and MICRO/T-11 chips, to the Falcon SBC and LSI-11/23, to the Winchester-based MICRO/PDP-11 system. Plus a huge range of boards and peripherals to go with them.



The MICRO/PDP-11 high-performance system for under $10,000.*

So we can honestly give you make/buy advice, without trying to sell you one approach over another.

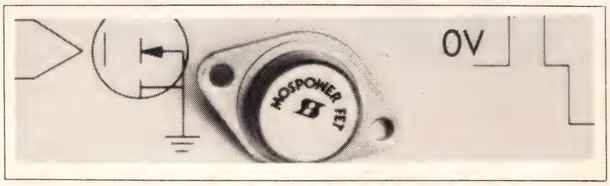
Better system performance.

Since we're the only major computer company that is also a major micro company, we can provide something other companies can't match: total system performance.

Like the minicomputer power you get from our RSX-11M-PLUS and the highly optimized code that's produced by our languages such as FORTRAN IV, COBOL, DIBOL, BASIC, and many others.

*U.S. Prices Only

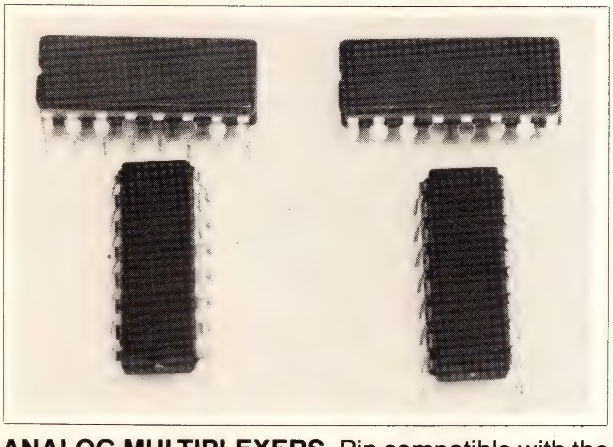
ICs & Semiconductors



PWM CONTROLLERS. Designed for driving MOSFETs and bipolar transistors in switching power supplies, PWM25 and PWM27 pulse-width modulators require only three external components. They contain the error amplifier, flip flop, oscillator, PWM and voltage regulator needed for controlling drive-signal frequency and pulse width. Each device provides two ±100-mA outputs: OFF state LOW (PWM25) or OFF state HIGH (PWM27). You can adjust dead time by connecting a resistor between two pins, and you can obtain drive frequencies to 400 kHz by choosing an external resistor and capacitor. The internal regulator maintains 5V±10 mV over the full input range of 8 to 35V; this 5V is also available for external loads to 20 mA. Housed in a 16-pin ceramic DIP, the devices operate over −25 to +125°C. $5.99 (100). **Siliconix Inc,** 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 290

ICs & Semiconductors



ANALOG MULTIPLEXERS. Pin compatible with the 508/509 MUXs, MP7508DI and MP7509DI dielectrically isolated CMOS devices provide 8-channel single-ended and 4-channel differential operation, respectively. Featuring overvoltage protection and direct TTL/CMOS interfacing, they come in a plastic DIP (0 to 70°C) or Cerdip (−25 to +85°C and −55 to +125°C) or in chip form. -883B processing is also available. $6.75 (100). **Micro Power Systems Inc,** 3100 Alfred St, Santa Clara, CA 95050. Phone (408) 727-5350.

Circle No 289

Are You a Current Battery Expert? Try this Designer's Quiz

Normally, Globe Battery Division is the leader in battery answers. In this case, we'll lead with some questions. See how you fare with this battery quiz.

Question 1—True or False:

When comparing two batteries of identical volumes but with different capacity ratings, the battery with larger capacity is probably a better battery.

Answer:

False. There is no correlation between capacity and quality. However, there is a correlation between capacity, volume and life. The rule of thumb is, the lower the capacity for a specific volume, the longer the life.

Higher capacity (rated AH) is achieved by increasing the amount of lead in the battery. Within a specific volume however, an increase in the amount of lead can only be accomplished by reducing the amount of electrolyte, resulting in premature failure due to recharge problems.

Question 2—True or False:

When testing identically rated batteries, initial capacity is not an accurate gauge of battery quality.

Answer:

True. Initial capacity is not a very good method of judging the quality of a battery. In some cases, manufacturers choose to improve the initial capacity of their batteries by lowering the paste densities. However in so doing, the shedding of plate material substantially decreases its cycle life. (See illustration below)

Globe Gel/Cells are designed for extended cycle life, while optimally meeting initial capacity criteria. Unsurpassed performance over the life of the cell, and extended cycle life is what sets Gel/Cell apart from the rest.

Question 3—True or False:

A "deep cycle" occurs when a battery is rapidly discharged to a very low voltage.

Answer:

False. Depth of discharge (or deep cycle) is determined by the percentage of rated capacity extracted from the battery. A deep discharge occurs when 80%-100% of the capacity is discharged, as in the case of a low current discharge over an extended period of time.

For example, reducing the voltage in an automotive battery to the point where it can't crank the engine is not a deep cycle. In actuality, only approximately 10% of the capacity has been discharged. However in the case of a battery driven wheelchair, where 70%-90% of capacity can be discharged during continued use, deep cycles are recurrent. When specifying batteries for deep cycle applications, be sure to get the percentage of capacity discharged during the tests. At Globe Battery Division, our data on cycle life is always based on minimum discharge depths of 85% of capacity.

Question 4—True or False:

Failure of batteries in float applications is usually caused by loss of electrolyte due to gassing during continuous charging.

Answer:

False. Electrolyte loss due to gassing contributes little to the potential failure mode of batteries in float applications. Actually, grids would corrode long before gassing could have any effect on the life of the cell. Therefore, the thickness of the grids has much more bearing on float life than gassing.

Question 5:

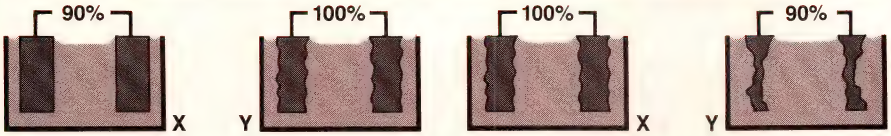
Is there a way for you to get more information on the implications of battery technology on your designs?

Answer:

Absolutely. Globe Battery Division would be pleased to schedule a seminar conducted by our engineers to provide you and your staff with more in-depth information. Information that can help you make better use of battery technology in your designs.

With 70 years of experience in lead acid battery technology, Globe Battery Division has established a tradition of providing knowledgeable assistance to design engineers. Call or write Mr. Robert Scrima at Johnson Controls, Inc., Globe Battery Division, Industrial Products Group, 900 East Keefe Avenue, Milwaukee, WI, 53201, (414) 228-2398.

How initial capacity can affect the cycle life of a battery.



After 1-5 cycles *After 100 cycles*

Battery Y shows a higher initial capacity because more plate surface is exposed to electrolyte—a result of increased irregularities in its surface (low density). However after 100 cycles battery X (high density) meets its rated capacity, while battery Y's capacity has deteriorated due to shedding of plate material. Look beyond initial capacity when testing a battery for your needs.

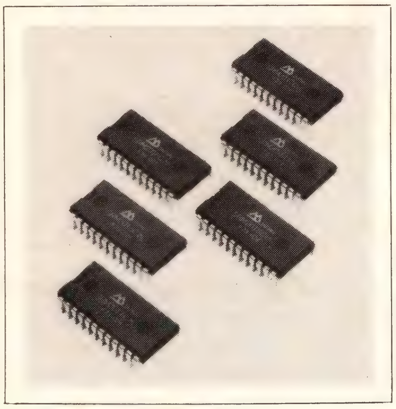
gel/cell®

Globe Battery Division

JOHNSON CONTROLS

CIRCLE NO 71

ICs & Semiconductors

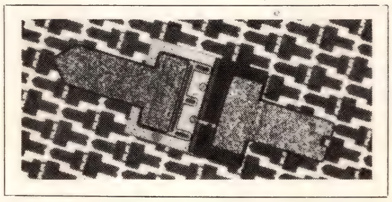


CMOS RAMs. Featuring pin compatibility with 2716-family EPROMs, Series SRM2016/2017/2018 fully static 16k CMOS RAMs require no clock or refreshing. Organized as 2048×8, they are TTL compatible and spec access times of 200 nsec max (-C20) or 250 nsec max (-C25). Using one 5V supply, the RAMs retain data with supplies down to 2V. They are packaged in a 24-pin plastic DIP; ceramic-DIP and Cerdip versions are also available. $9 (100). **Epson America Inc,** 3415 Kashiwa St, Torrance, CA 90505. Phone (213) 534-0360. TLX 182412.

Circle No 291

REAL-TIME CLOCK. Operating as a peripheral device with CDP1800 Series and most other nonmultiplexed-bus μPs, the CMOS CDP1879 IC features time-of-day/calendar outputs, alarm circuitry, time-of-day interrupts and a power-down mode. It includes five programmable counters that divide down an external oscillator input to provide time and calendar information from seconds to months in BCD format. Alarm circuitry can be set for seconds, minutes or hours to activate the Interrupt output when the alarm registers match those of the counters. Interrupts can be generated by the alarm circuits or one of 15 selected clock signals that range from subsecond to day-length interrupts. Operating at one of four different crystal frequencies (32,768 Hz and 1.04, 2.09 or 4.194 MHz), the device provides a separate clock output that selects one of 15 50% duty-cycle outputs to be sent to the μP. $9.05 (100) for 5V, 24-pin plastic-packaged version. **RCA Solid State Div,** Box 3200, Somerville, NJ 08876. Phone (201) 685-6319.

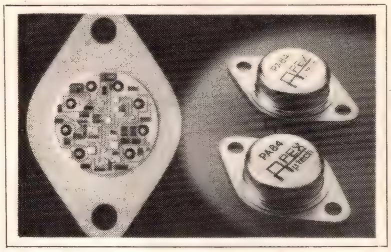
Circle No 292



BEAM-LEAD SCHOTTKY DIODES. Available in low- or medium-barrier versions, Series HSCH-5300 microwave diodes offer a choice of three capacitance values. Typically used in mixers and detectors, they exhibit repeatable RF characteristics through the Ku band. A special process yielding large support areas results in strong beams—6g typ lead pull—without compromising capacitance (0.10 pF typ). The devices' metallization system produces a Schottky junction stable to 300°C, seals the passivation-system junction and anchors the gold-plated beams to the die. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 293

OP AMPS. Furnishing improved gain-bandwidth product, slew rate and output-current capability, Models PA84/84A are pin compatible with the Burr-Brown 3584JM. They feature 75-MHz



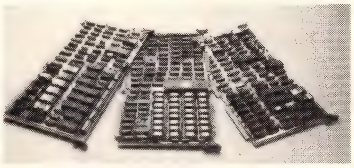
gain-bandwidth and 200V/μsec slew rate and deliver 290V p-p max output with load current of ±40 mA. The devices are protected by overtemperature circuitry as well as short-circuit current limiting, and their input stage can withstand differential input voltages equal to the power-supply levels. FET inputs keep bias currents as low as 5 pA (PA84) or 3 pA (PA84A); offset drifts equals are 10 μV/°C (PA84) and 5 μV/°C (PA84A). Operating from supplies of ±15 to ±150V, the devices use thermally efficient beryllia substrates and aluminum wires to provide high power dissipation. $66.50 and $77.50 (100), respectively, for the PA84 and PA84A. **Apex Microtechnology Corp,** 1130 E Pennsylvania St, Tucson, AZ 85714. Phone (602) 746-0849.

Circle No 294

A-LAW CODEC. Pin and function compatible with the 2911A, TCM2911A provides the A/D-D/A interface, A-Law companding and decoding logic needed for a voice-band communications channel. Although it performs 8-bit conversion, its companding feature yields 12-bit dynamic range. Operating from +12 and ±5V supplies, the device consumes 230 mW while operating and 33 mW in power-down mode. It comes in a 22-pin ceramic DIP. $11.62 (100). **Texas Instruments Inc,** Box 202129, Dallas, TX 75220. Phone local office.

Circle No 295

Computer-System Subassemblies

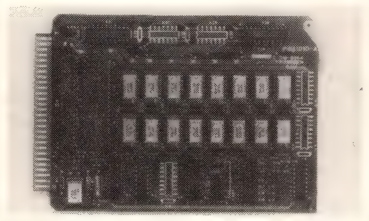


MULTIBUS BOARDS. These CPU, main-peripheral, video and serial-I/O boards provide complete 68000-μP capability and can be easily integrated into Multibus systems. The CPU board has 256k bytes of on-board RAM that permits the μP to execute code at full speed (8-MHz clock with no Wait states). Bus-timeout and simple memory protection as well as interrupt-type selection are provided. The main-peripheral unit features 32k bytes max of PROM, a triple interval timer, two programmable USARTs, an error-polynomial generator and checker, three parallel-interface chips, a keyboard interface, a baud-rate generator for the USARTs and a priority interrupt controller. Incorporating 32k bytes of RAM, a programmable video controller and a programmable DMA controller, the video board provides as many as 256 PROM characters. The serial-I/O board furnishes as many as five serial I/O ports, an interface to a bar-code wand and an interface to a proportional-spacing printer. From $700 (50). **TSD Display Products Inc,** 35 Orville Dr, Bohemia, NY 11716. Phone (516) 589-6800. TLX 144659.

Circle No 274

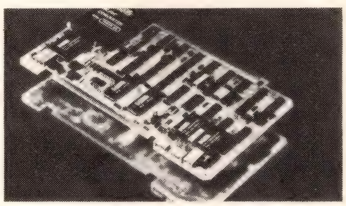
WINCHESTER CONTROLLER. The ACS-500 Series comprises five LSI chips: four proprietary devices and an EPROM containing the microcode for operation in a SASI (Shugart Associates System Interface)-bus environment. They provide all Winchester-drive control and handling functions and are divided into logical blocks including the encode/decode function for MFM, sequence and serialization/deserialization logic, a combination voltage-controlled oscillator and phase-locked loop, and a dual-ported buffer control that permits FIFO-type multisector buffering for high-speed throughput. One channel operates with multiple hosts or multiple controllers; transfer rates reach 10M bytes/sec. $190 (1000); controller boards, $350 (500). **Adaptec Inc,** 1625 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 946-8600.

Circle No 275



DYNAMIC RAM. Available in 64k-byte (Model 6064) or 128k-byte (Model 6128) configurations, Model 6064/6128 contains an on-board refresh controller for processor independence. The STD Bus unit provides optional parity generation/checking. A parity error generates a non-maskable interrupt by asserting the NMIRQ signal on the STD Bus. Two addressing modes (16 and 20 bit) are available, and the RAM board uses the STD-8088 address-expansion technique, in which the most significant address bits are multiplexed over the data bus at the beginning of a memory cycle. Model 6064, $490; Model 6128, $690; with parity option, $530 and $750, respectively. **Systek,** 6515 W Clearwater Ave, Suite 222, Kennewick, WA 99336. Phone (509) 735-1200.

Circle No 276

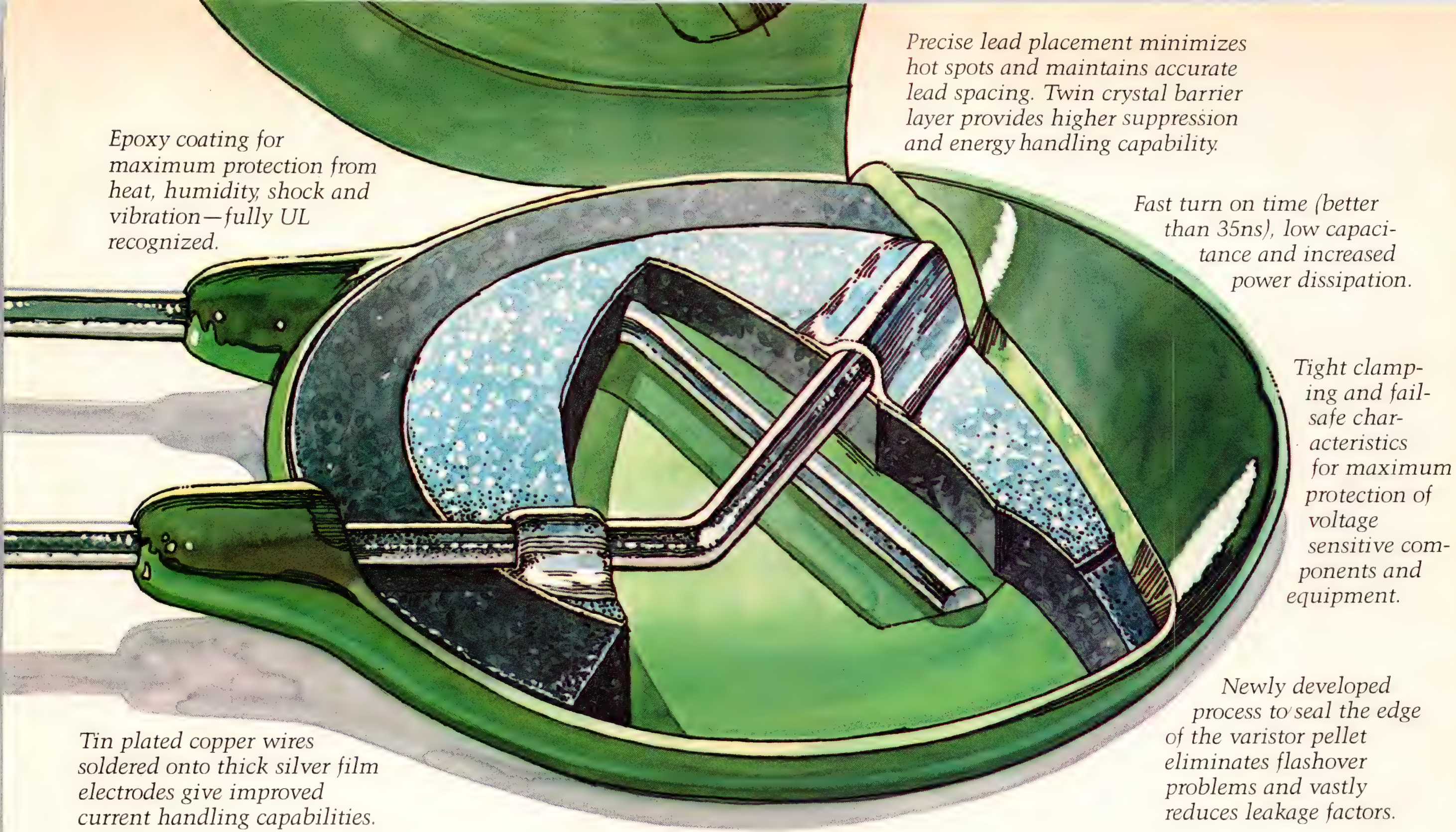


ANALOG-I/O BOARD. For Motorola Exorciser systems and Rockwell System 65 μCs, SineTrac ST-6832 accepts as many as 32 single-ended or 16 differential analog-input channels. Under μC program control, it selects, digitizes and stores the data in user-selected memory locations. Two D/A channels are available for data distribution. A memory-mapped device, the unit is organized around eight consecutively addressed registers with a user-selectable base address. For real-time applications, an on-board Pacer real-time clock is included, frequency selectable under program control. A ±15V dc/dc converter supplies voltage to the linear circuitry from the 5V Exorciser power supply. From $689 for 32 A/D channels and instrumentation-amp gains of 1, 2, 4 and 8. **Datel-Intersil,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-9341. TWX-710-346-1953.

Circle No 277

A/D CONVERTER. Taurus high-resolution μP-compatible converter features ±16- or ±17-bit resolution, ±100-mV or ±1V user-selectable input signals and a conversion rate of 20 per sec. STD Bus compatible, it provides sign-magnitude binary output. Operating temperature spans 0 to 70°C, and the unit requires ±15V at 50 mA and 5V at 300 mA. $605. **Lincoln Instruments Inc,** 456 W Montana St, Pasadena, CA 91103. Phone (213) 798-0733.

Circle No 278



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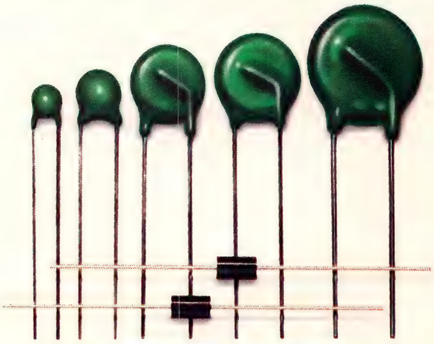

STETRON

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Tlx: 206-742

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CIRCLE NO 73

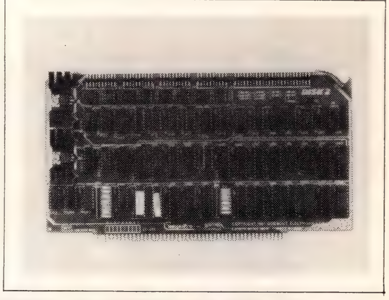
Computer-System Subassemblies

CONTROLLER/INTERFACE. A single-board Multibus-compatible unit, the DSD 5215 simultaneously interfaces to 5¼-in. Winchester, ¼-in. streaming-tape and 5¼-in. floppy-disk drives. It features advanced architecture with a high-speed internal bus for pipelining of data, 24-bit addressing, noninterleaved data transfer, an on-board data separator and on-board 32-bit error-correction code. The device emulates Intel's iSBC 215 and iSBX 218 controllers and thus provides software compatibility with Intel's RMX 86 operating system. It interfaces to low-cost Seagate and Tandon drives. A phase-locked loop performs data separation for the Winchester and floppy disks, and a proprietary ECC chip can generate both Winchester ECC and cyclic redundancy check for the floppy disks. $2200. Delivery, 30 to 45 days ARO. **Data Systems Design,** 2241 Lundy Ave, San Jose, CA 95131. Phone (408) 946-5800. TWX 910-338-0249.

Circle No 279

I/O SYSTEM. Intelligent Data Acquisition and Control chassis (IDAC) uses an integrated 16-bit μC to control industrial automation configurations of as many as 4800 digital and analog I/O lines. It can serve as a stand-alone-sensor I/O system or a node in a distributed-sensor I/O network. As a stand-alone system, it can be configured with a CRT terminal, dual diskettes or Winchester disk and medium-speed printer. This system can process real-time data, control processes, generate reports and maintain test or process histories. In a distributed network, several chassis can control different parts of complex processes; a host CPU provides overall system management. The chassis is programmed for individual tasks and has five slots; another 12 are available for any combination of DG/DAC Sensor I/O Library cards, which include analog I/O, TTL and non-TTL digital I/O, high-speed A/D and D/A converters, analog multiplexers, relay cards and optically isolated digital-I/O and triac modules. With 32k to 64k bytes of memory and no terminal boards, $6850 to $7150. **Data General Corp,** 4400 Computer Dr, Westboro, MA 01580. Phone (617) 366-8911.

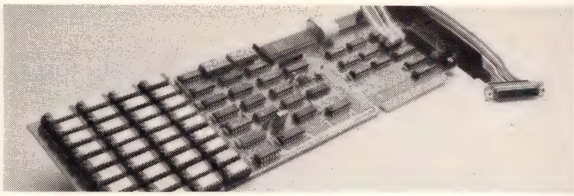
Circle No 280



DISK CONTROLLER. Capable of directly accessing a 16M-byte address space by means of a Burst-mode DMA interface, the 696/S-100-bus Disk 2 provides processor-independent data transfer between system memory and as many as four Winchester 8- and 14-in. disk drives. Interfacing to Shugart SA4000 Series, Fujitsu 2300 Series and Memorex 101 Series drives, it is fully compatible with the MP/M, OASIS, CP/M-80 and CP/M-86 operating systems. Providing 24-bit addressing transferred across 64k boundaries, the unit has an I/O-mapped interface that permits contiguous system memory and 16 switch-selectable arbitration priority levels. $795. **CompuPro Systems,** Oakland Airport, CA 94614. Phone (415) 562-0638.

Circle No 281

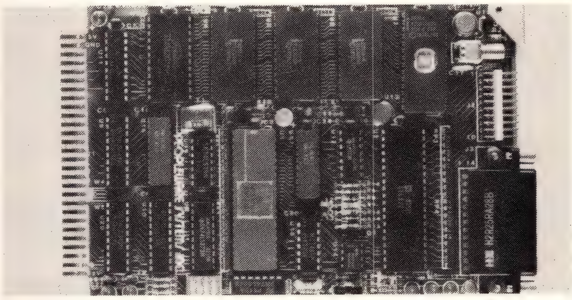
Computer-System Subassemblies



COMPUTER BOARD. The Quadboard combines four IBM Personal Computer boards into one, leaving slots for further expansion. Compatible with IBM hardware, it includes 256k-byte memory expansion, a clock/calendar, parallel printer I/O and an asynchronous (RS-232) communications adapter. Memory is expandable in 64k-byte increments. Full parity generation and checking come standard; parity can be switch disabled to avoid system lock-up upon error detection, and DIP switches provide addressing starting on any 64k block. The asynchronous communications adapter is software programmable for baud rate, character and stop and parity bits and uses the same chip as the IBM async board. With 64k of RAM, $595; 128k, $775; 192k, $895; 256k, $995. **Quadram Corp,** 4357 Park Dr, Norcross, GA 30093. Phone (404) 923-6666.

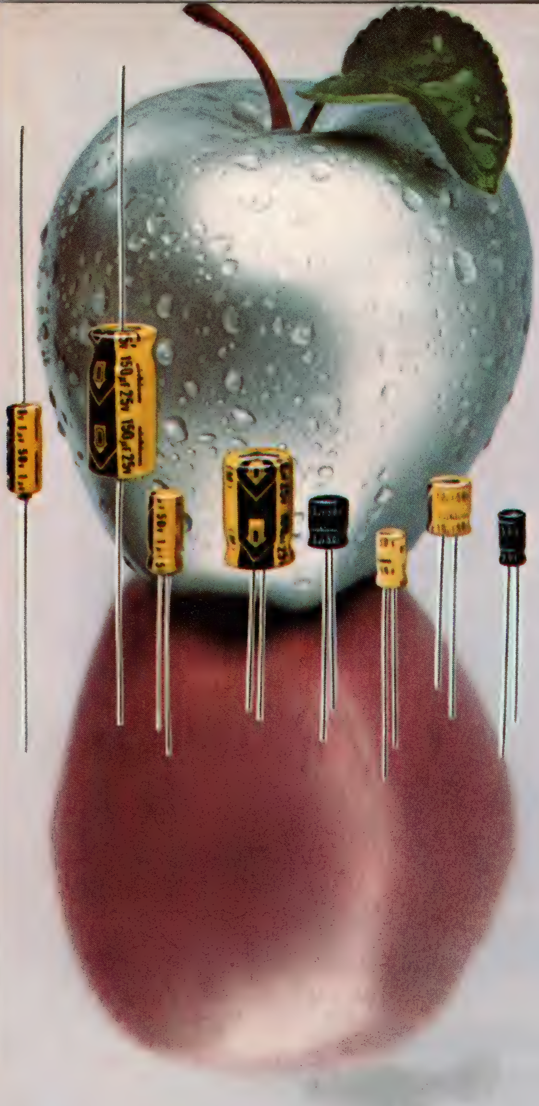
Circle No 282

Computer-System Subassemblies



SINGLE-BOARD μC. The P-Forth card incorporates a FIG FORTH firmware package and built-in EEPROM. STD Bus compatible, it permits programming into nonvolatile memory; as soon as the application is verified and functioning, the program becomes available via a switch on the card. Upon power-up, the card then runs the application directly. Based on the 6801 μP, the μC includes an editor for use in developing applications, an assembler to permit writing of assembly-language routines and a monitor for debugging. It accepts 16 I/O bits and also furnishes a programmable timer and an RS-232 interface. $645. **Peopleware Systems Inc,** 5190 W 76th St, Minneapolis, MN 55435. Phone (612) 831-0827.

Circle No 283



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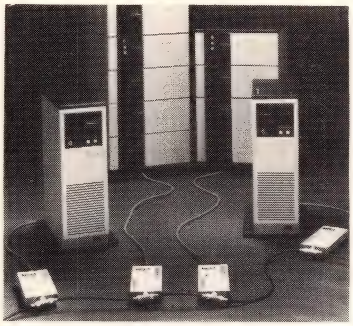
Series Type	Lead Style	Series Features	Body Diameter (Range in Inches)	Body Length (Range in Inches)	Rated Voltage Range (V.DC)	Capacitance Range (μF)
TKB	Axial	Very low leakage Replaces tantalum capacitors Miniature size	0.196 ~ 0.393 5 ~ 10 mm	0.472 ~ 0.827 12 ~ 21 mm	6.3 ~ 100	0.47 ~ 100
UKB	Radial	Very low leakage Replaces tantalum capacitors Miniature size	0.196 ~ 0.393 5 ~ 10 mm	0.433 ~ 0.787 11 ~ 20 mm	6.3 ~ 100	0.1 ~ 100
SA	Radial	Superminiature size Standard 7 mm body length Low leakage Replaces tantalum capacitors	0.157 ~ 0.248 4 ~ 6.3 mm	0.275 7 mm	6.3 ~ 63	0.1 ~ 100
SL	Radial	Superminiature size Very low leakage Standard 7 mm body length Replaces tantalum capacitors	0.157 ~ 0.248 4 ~ 6.3 mm	0.275 7 mm	6.3 ~ 63	0.1 ~ 100

CIRCLE NO 77

Computers & Peripherals



COMPUTER SYSTEMS. System 8000 Models 10, 11, 21 and 31 provide 8- to 24-user capability and include a common CPU board (based on the 6-MHz Z8001A processor, which supports eight serial I/O ports and a parallel I/O port) and peripheral controllers. Utilizing ZEUS operating-system software, they support high-level languages such as FORTRAN, C, PASCAL and BASIC; high-speed local-area-network communication occurs via the manufacturer's Z-NET II option. Measuring 8×28×18 in., Model 10 comes with 256k bytes of parity memory, a 5¼-in. Winchester disk with 18M-byte storage capacity and a 1M-byte floppy-disk drive for backup. Model 11 adds a 17M-byte cartridge tape drive and an intelligent Z80B-based tape-cartridge controller board. The 33×19×24-in. Model 21 furnishes a standard 10-slot card cage and 1M bytes of error-correcting memory, an 8-in. Winchester disk with 32M-byte storage capacity and a 17M-byte cartridge tape drive for backup. Model 31 substitutes an 80M-byte SMD-compatible Winchester disk drive for Model 21's Winchester, providing 320M-byte max storage capacity. Model 10, $13,950; Model 11, $16,950; Model 21, $29,950; Model 31, $40,000. **Zilog Inc,** 1315 Dell Ave, Campbell, CA 95008. Phone (408) 370-8000. TWX 910-338-7621.

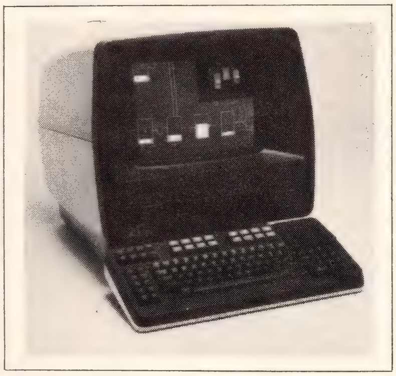
Circle No 552

COMPUTER SYSTEM. Incorporating Z80 and 8088 μPs and offering several operating systems (including CP/M, MS-DOS and OASIS), the Vector 4 comes in two models. Model 4/20 is a dual-floppy-disk-drive system with 630k-byte capacity on each 5¼-in. disk. Model 4/30 has one floppy-disk drive with 630k-byte capacity and a Winchester drive with 5M-byte capacity. The system utilizes the 16-bit μP's power, while running 8-bit software, by calling on 16-bit commands to speed up selected 8-bit programs. For example, under the extended CP/M operating system, the 8088 handles disk transfers four times as fast as the Z80. The system provides 128k of main memory, expandable to 256k. Memory-mapping logic allows the Z80 to access the entire memory in increments as small as 2k. Main memory is time shared between the CPU and the video-display controller. Model 4/20, $4495; Model 4/30, $5995. **Vector Graphic Inc,** 500 N Ventu Park Rd, Thousand Oaks, CA 91320. Phone (805) 499-5831.

Circle No 551

GRAPHICS TERMINALS. Available in two versions for business and two for technical applications, HP 2700 Series units offload graphics calculations from a host computer, display multiple views using zoom and

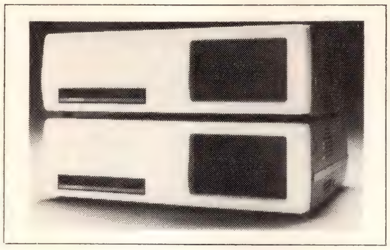
CIRCLE NO 78 →



pan capabilities and simultaneously exhibit 16 of 4096 colors on the screen. By storing a vector list, the devices allow you to pick, move, scale or rotate an object using local graphics manipulation. Multiple views can be displayed through as many as 255 windows on the screen. 32k×32k addressable resolution provides a vector workspace of more than one billion addressable points. Combining additional vector memory and cursor control via a graphics tablet, Model 55 becomes an extension to a host-driven CAD package. Model 60 utilizes AUTOPLOT/2700 software to permit creation of pie, bar, linear or log charts and addition of graphics text to annotate those charts. Model 65 provides freehand sketching, aided drawing and picture editing via PAINTBRUSH/2700 software. Model 50, $19,900; Model 55, $24,000; Model 60, $24,000; Model 65, $28,000. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

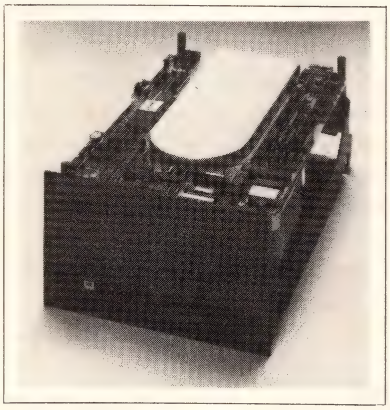
Circle No 553

STAT MUXs. Available as basic 4-channel units with one data link, NES statistical multiplexers can be incremented with 4-channel modules to concentrate as many as 32 lines into one high-speed data link (an optional backup data link is also available). The NES9100 and the NES9200 (a unit that incorpo-



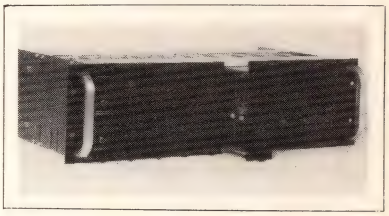
rates individually designated port switching, port selection and contention features) are compatible with their manufacturer's 90/10 Network Control and Management System and 90/15 Performance Measurement System. Transparent to users while operating the high-speed data link, they function at input speeds to 9600 bps and handle data from a group of terminals with an aggregate data rate two to four times higher than the data-link speed. Each input data line independently configures to handle asynchronous or optional bisynchronous data. Autobaud is a standard feature, guaranteeing that the port rate automatically matches the device connected for dial-up inputs. NES9100, $2550; NES9200, $3050. **Intertel,** 6 Shattuck Rd, Andover, MA 01810. Phone (617) 681-0600.

Circle No 554



WINCHESTER DRIVES. Models 3046, 3033 and 3020 5¼-in. drives supply 46.3M, 33.7M and 19.8M bytes of unformatted storage, respectively. Providing 30-msec access time, they use four, three and two 130-mm-diameter oxide-coated disks mounted within a common housing. Interchangeable with standard 5¼-in. floppy-disk drives, the units employ a closed-loop servo equipped with a linear actuator and Winchester-type ferrite read/write heads. They weigh 6.5 lbs and can be mounted horizontally or vertically. Drives spec 3-msec track-to-track access time, 8.3-msec average latency and 3-msec settling time. Mean time between failures equals 10,000 power-on hrs. 3033, $1800; 3020, $1470 (1000). **Atasi Corp,** 235 Charcot Ave, San Jose, CA 95131. Phone (408) 942-0770.

Circle No 555



INTELLIGENT CONTROLLER. For industrial and process-control applications, Model CS105 services a variety of I/O devices and standard buses (including STD, IEEE-488 and CAMAC) and acts as a master/slave in systems utilizing those buses. Its hardware is contained in pluggable modules enclosed in a metal subchassis. A central module contains a printer interface, real-time clock, host/target switch to move to and from Program Development mode, protected programming switch for EEPROMs and ac isolated power control for external power supplies. A CPU module utilizes the 8085A μP and contains bus-interface circuitry, an RS-232C port and a cassette-memory interface. The device services as many as four 16k memory modules: Module 1 holds 16k of EPROM with BIOS

and the FORTH nucleus; module 2 contains 6k of system RAM, 2k of EPROM for patching, 4k of EPROM for screens 0 to 3 with error messages and editor functions and 4k of RAM for user-available screens 4 to 7; and modules 3 and 4 are available for additional user screens. Supplied with 8085 FIG FORTH, the unit includes a FORTH decompiler, an 8085 assembler, a portable line editor and a screen-oriented editor. $2995. **Controlex Corp,** 16005 Sherman Way, Van Nuys, CA 91406. Phone (213) 780-8877.

Circle No 556

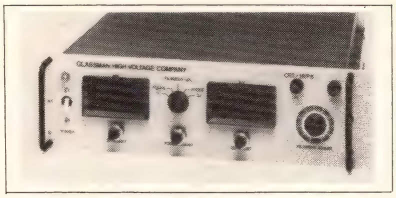
COMPUTER WORKSTATION. The Unistar 100 consists of the CD100M Multibus-compatible workstation with 10M-byte 5¼-in. Winchester and 0.6M-byte floppy-disk drives, a 12-in. P31-green-phosphor CRT, a detached keyboard and an ANSI-compatible video controller. Its 68000 CPU runs at 8 MHz and employs 256k bytes of dual-port local memory, expandable to 1M bytes. Local memory ensures that the 68000 avoids Wait states. Optimized for 16 users, the unit features 2-level memory-management hardware with fast-process context-switch capability and such exception-processing capabilities as parity, five system timers, page map, segment map and system-space facilities. Two RS-423 multiprotocol serial ports and a parallel 16-bit I/O port ease I/O. The system also provides a workstation for running the Bell Labs UNIX operating system. **Callan Data Systems,** 2645 Townsgate Rd, Westlake Village, CA 91361. Phone (805) 991-9156.

Circle No 557

VIDEO DISPLAY TERMINAL. Visual 50 displays 24 80-character lines on a 12-in. screen and provides 7×9 dot-matrix characters, a 128 ASCII character set and blink, reverse-video, underline, aim and blank attributes. It furnishes menu-selectable emulation of the Hazeltine Esprit, ADDS Viewpoint, Lear Siegler ADM-3A and DEC VT52 units; an RS-232C interface allows communication with a variety of host-computer systems. The unit comes in a plastic housing and provides tilt-and-swivel capabilities, a detached low-profile keyboard and matte-finish keycaps. Other features include menu-style setup modes (in nonvolatile memory), 25th status line, a line-drawing character set for charts and graphs, and smooth scrolling. Options include international character sets in eight languages and a P31-green-phosphor display. $695. **Visual Technology Inc,** 540 Main St, Tewksbury, MA 01876. Phone (617) 851-5000.

Circle No 558

Instrumentation & Power Sources

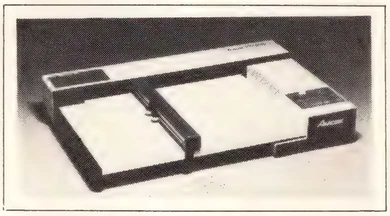


CRT SUPPLY. The 4-supply CRT-HVPS provides output voltages for G1, G2, focus and filament circuits. It interfaces with one of its manufacturer's 19 LG or HG supplies, and the 5-supply combination fits in two 5¼-in. racks. Two large panel meters provide a switch-selectable LED display of all voltage and current outputs. Oscillator-rectifier circuitry protects against overload, and high oscillator frequency permits ripple as low as 0.1%, with minimal stored energy. Efficiency at full load specs at >75% typ, and recovery time from a 50% load transient equals <5 msec. $1895. Delivery, stock to 8 wks ARO. **Glassman High Voltage Inc,** Box 551, Whitehouse Station, NJ 08889. Phone (201) 534-9007.

Circle No 284

ANALOG RECORDER. Producing hard-copy data describing the relationship between two analog variables or one analog variable and time, Model 60000 incorporates X and Y input amplifiers with floating and guarded inputs that exhibit a constant impedance of 1 MΩ for minimal source loading. Eighteen calibrated sensitivities from 50 μV/cm to 20V/cm (variable between steps) accommodate a wide range of input signal amplitudes, and for Y-T recording, the timebase provides eight calibrated X-axis speeds from 0.1 to 20 sec/cm. Slewing speed equals 134 cm/sec. Silent electrostatic paper holddown and edge lights ease positioning of 8½×11-in. paper, and a muting facility removes the drive from both servo motors, allowing manual movement of the pen carriage to any position on the bedplate. $2200. Delivery, 6 wks ARO. **Gould Inc,** Instruments Div, 3631 Perkins Ave, Cleveland, OH 44114. Phone (216) 361-3315.

Circle No 285

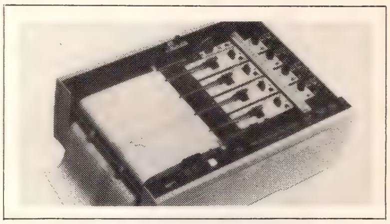


4-COLOR PLOTTER. Model DXY provides a 10×14-in. effective plotting range, plotting speed of 2.73 ips max and step size of 0.003 in./step. A Centronics interface eases connection to a computer. The 4-color unit's Control command and Basic command permit drawing of figures; four pens, pen holders and chart hold-downs come standard. Functions are expandable via added ROM. $949. **Amdek Corp,** 2420 E Oakton St, Suite E, Arlington Heights, IL 60005. Phone (312) 364-1180.

Circle No 286

DRAFTING PLOTTER. For IC and pc-board design, generation of electrical schematics, mechanical-parts design and facilities layout, the μP-controlled HP 7585A features 4g acceleration and speeds to 24 ips. Pen-handling capabilities include automatic setting of pen force and writing speed, automatic capping of pens not in use and programmed selection of as many as eight pens for combining color, line width and pen type on one plot. As many as seven internally stored line types can be specified: solid, dotted, dashed and combinations of dotted and dashed; the μP automatically scales each line pattern between vector endpoints to provide uniform line-style appearance and output quality. Addressable resolution specs at 0.001 in., mechanical resolution, 0.00012 in. and repeatability, 0.002 in. $22,750. Delivery, 9 wks ARO. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 287



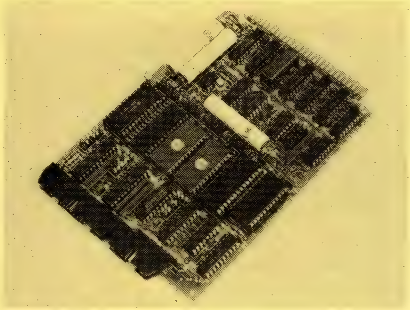
OSCILLOGRAPHS. 8K20 Series rectilinear thermal-writing chart recorders feature frequency response to 105 Hz and use long-life thermal pens. They come with 40- or 80-mm galvanometers in mainframes of two to 12 channels. Three types of input preamplifiers are available: high gain, low gain and direct fixed range, with sensitivities from 0.5 mV/cm to 200V/cm. Paper speeds are selectable from 500 mm/sec to 1 mm/min; timing intervals equal 0.1 or 1 sec and 0.1 or 1 min. Several recorders slaved to a master unit using the timing-signal output increases the number of channels recorded synchronously. Automatic electronic overrange protection, event marker, simultaneous pen lift and provision for roll or z-fold chart paper are standard, as are remote control of chart drive, pen heat on/off and paper-drive synchronizer. From $3475. **Soltec Corp,** 11684 Pendleton St, Sun Valley, CA 91352. Phone (213) 767-0044.

Circle No 288

EDN PRODUCT MART

This advertising is for new and current products.

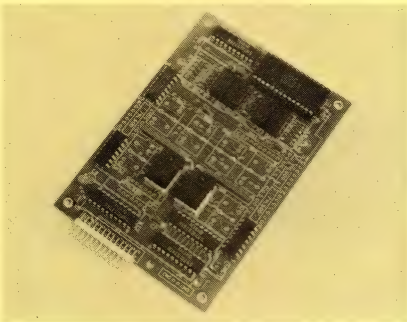
Please circle Reader Service number for additional information from manufacturers.



The DSTD-703 is a multi-function Calendar Clock module compatible with the STD BUS architecture. The DSTD-703 provides full calendar clock capability with 1/10000, 1/100, sec, min, hour, day/week, day/month, month, 4 byte wide sockets for CMOS RAM, full battery backup, 16 bit bi-directional parallel port, CTC interrupt and brown-out detection. The DSTD-703 occupies 4 I/O port location.

For more information contact:
dy-4 Systems Inc., Marketing Department
888 Lady Ellen Place, Ottawa, Ont. Canada
Tel.: 613-728-3711

CIRCLE NO 90

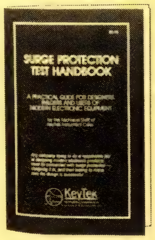


DSTD-ACC-RDSM is a remote display module used in conjunction with the DSTD-703, STD BUS Calendar Clock card providing up to 8, 7 segment displays and 8 fully debounced switches with integral leds, the DSTD-ACC-RDSM interfaces to the DSTD-703 over the parallel port provided.

For more information contact:
dy-4 Systems Inc., Marketing Department
888 Lady Ellen Place, Ottawa, Ont. Canada
Tel.: 613-728-3711

CIRCLE NO 91

IC's HATE SURGES

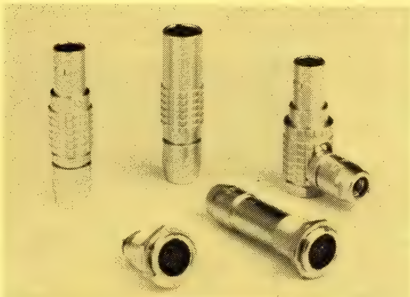


How well are your circuits & systems protected against transient voltage and current surges? This new, fully-illustrated, 64-page handbook tells you how to find out for sure. It is a definitive guide to the surge protection and testing of systems, circuits and protective devices for surge vulnerability. Includes detailed coverage of new IEEE Std 587-1980 for ac power-line spike surges and other significant surge standards, as well as the latest in surge test equipment. **A must for designers and users of modern, IC-based electronic equipment.**

Price: $3.75/copy — Order from:

KeyTek Instrument Corporation
12 Cambridge Street
Burlington, MA 01803
(617) 272-5170

CIRCLE NO 92

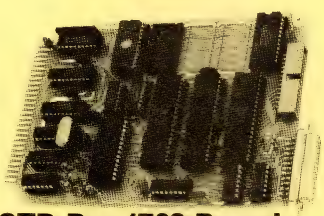


LEMO SELF-LOCKING CONNECTORS

New Lemo B Series self-locking cylindrical connectors incorporate a shell-based guide and keyway polarization system. The result is an extremely rugged, high density, multi-contact connector which is aesthetically very attractive and which is easy to engage and disengage. Connectors are initially available in four shell sizes with from 2 - 30 contacts.

Lemo U.S.A. Inc.
P. O. Box 6626
Santa Rosa, CA 95406
(707) 523-0600

CIRCLE NO 93



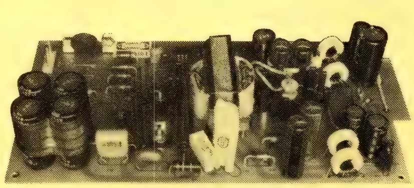
STD Bus/Z80 Based RS 232C/Two Parallel I/O

All the above and more on one 4-1/2 x 6-1/2 board! Up to 8K EPROM (2K furnished) and 2K RAM, furnished. 110-9600 baud software selectable with monitor program included. I/O connectors are on the board. Ideal for the heart of dedicated test sets or process controllers. Delivery of small quantities from stock. Use Visa, Mastercard or corporate purchase order.

MS 1002 (2 MHZ) $289.00
MS 1004 (4 MHZ) $314.00
Quantity prices available

ELTEC
Electrotechnics Corporation
P.O. Box 9308 Shreveport, LA 71109
Phone (318) 636-0563

CIRCLE NO 94



LOW COST 65 WATT SWITCHER

- Up to 5 Outputs
- 5 x 9½ x 2½" Size
- 110/220 VAC Input
- Overvoltage Protection
- Soft Start
- High Reliability
- Short Circuit Proof
- 50°C Temp. Ratings

Typical configuration, such as 5V @ 6A, 12V @ 1A, 12V @ .5A and 24V @ 1A is priced at $139.00 for a single unit and delivery stock to 8 weeks.

SWITCHING POWER INC.
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516-981-7231

CIRCLE NO 95

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CUSTOM IC'S

PROVIDE:

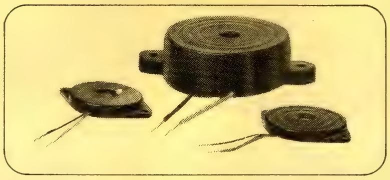
- Low Cost
- Low Power
- High Performance
- Small Size

We are able to design and provide low cost custom IC's for most applications. The use of semi-custom process allows these advantages for production runs as low as 1000 units.

For more information provide a brief description of your requirements.

MASS CIRCUITS, INC.
P.O. BOX 162, E. WALPOLE, MA 02032

CIRCLE NO 96

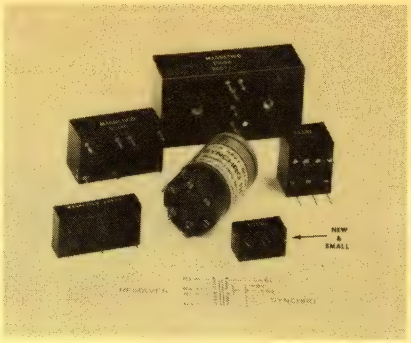


Sound advances. AT-12, 13 and 14 are Piezo Ceramic Transducers that deliver big sound at low cost. Get 57 dBA within a combined frequency range of 2.5 to 7.5 KH_z. Features: flange mounting with wire leads, voltage range of 1 to 30 Vp-p, operating temperature of -20°C to 60°C. High efficiency, reliability and low current drain. Contact:

Projects Unlimited, Inc., 3680 Wyse Rd.
P.O. Box 1426,
Dayton, Ohio
45414
(513) 890-1918

projects® unlimited

CIRCLE NO 97



400HZ INPUT SCOTT T—Synchro 3 wire input, L-L; Sine & Cos output; Part #10472 is 11.8 to 6v, 3/4 X 1-1/2 X 3/8; #13530 is 11.8 to 1v, 5/8 X 1-1/4 X .3; #50460 is 90 to 6v, 7/8 X 1-5/8 X 11/16; #13241 is 11.8 to 5v, .85 X .85 X 7/16; #52975 is 11.8 to 1v, 1/2 X 7/8 X 7/16 hi. No burn-out due to hi common mode surges, eliminates system grounding problems. Repeatable and interchangeable performance—no aging. Use for synchro-digital conversion encoders.—**Magnetico Inc.,** 182 Morris Ave., Holtsville, N.Y. 11742—516-654-1166. Call us for our complete line of Scott T's.

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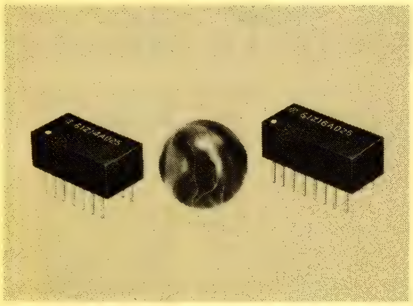
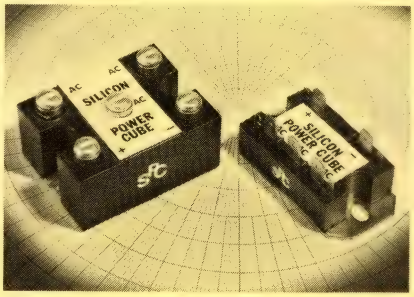


TAPPED DELAY LINES. Active digital Type 61Z provide precise tapped delays. Buffered TTL compatible input and output circuitry with compensation for propagation delay and internal loading. 5 tap intervals of equal delay. Total delay times, 25 to 500 nanoseconds; rise time (max.), 4 nanoseconds. Write for Bulletin 45005. **Sprague Electric Company,** 491 Marshall St., North Adams, MA 01247. (413) 664-4411.

CIRCLE NO 99



SPC POWER RECT. MODULES ARE UL RECOGNIZED.

These 25-40A & 50-100A encapsulated power rectifier modules come in 7 circuit choices: single & 3-phase bridges, 3-phase common anode & cathode and ½-wave center-tap versions, and diode-doublers. Their advanced unitized structures assure maximized thermal transfer and long term reliability. Up to 1200VRMS. Prices that start at $10 make them ideal for space, cost and time savings power conditioning applications.

SILICON POWER CUBE CORP.,
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(213) 634-9390

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IEEE 488 for STD bus

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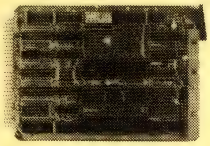

the Single Board GPIB Computer

featuring: 8085 CPU, RAM, ROM, 2-RS232, GPIB and development monitor.

For information, write or phone
Ziatech Corporation
3433 Roberto Court
San Luis Obispo, California 93401
(805) 541-0488

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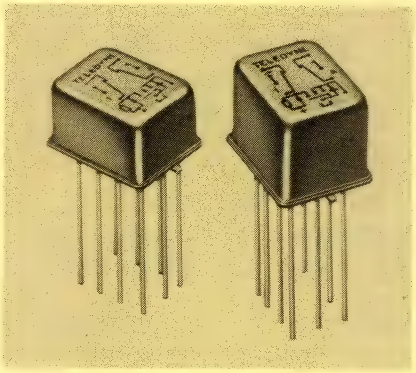

CMOS DRIVEN ELECTROMECHANICAL RELAYS

Teledyne's 116C general purpose, and 136C sensitive relays contain an integral power FET driver to allow relay operation directly from CMOS level signals. Hermetic package also houses Zener protection diode, coil suppression diode and DPDT relay which utilizes Teledyne's proven TO-5/Centigrid® design. Relay features .100 grid lead spacing, dry circuit to one amp contact rating, and excellent RF characteristics up through UHF. Standard coil voltages are 5V, 6V, 9V, 12V, 18V and 26.5V. Complies with MIL-R-28776. **Teledyne Relays,** 12525 Daphne Ave., Hawthorne, Ca. 90250 (213) 777-0077

CIRCLE NO 103

Panel Components Corporation International Primary Circuit Components 1982-83 Catalog and Designers Reference

New 1982-83 catalog and design reference contains detailed descriptions of primary circuit components with international and North American product safety approvals. Primary circuit connectors, RFI filters, international cords and cordsets, international plugs, sockets, and socket strips are covered. Each product section is preceded with a description of applicable international standards and requirements. Suggested guidelines for specifying each component type are also included.

Panel Components Corporation, P. O. Box 6626
Santa Rosa, CA 95406, (707) 523-0600

CIRCLE NO 104

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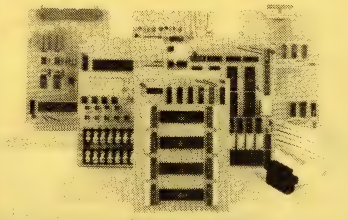
Joanne Dorian, (212) 949-4445 or **Diane Turco, (212) 949-4447**

6800 Micro Modules



FOR INTERFACING TO: sensors, transducers, analog signals, solenoids, relays, lamps, pumps, AC motors, DC motors, stepper motors, keyboards, displays, 488 GPIB.

ADDITIONAL FEATURES: 6800 MPU, counter/timer, fail safe battery back up

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Wintek Corp.
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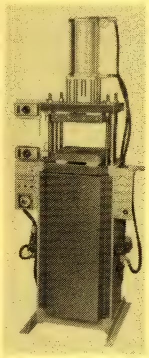
ENCAPSULATE

BY TRANSFER MOLDING



In epoxy, silicone or other thermoset. Our presses serve since 1964 in the production of DIP and other insert molded components. Highly economical 5 to 60 tons. Quiet & clean operation. Tooling & turnkey packages available.

Phone Bill Gluck
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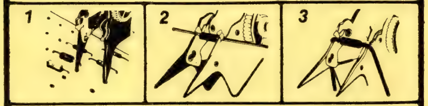
GLUCO, INC.

Box 336, Monroeville, PA 15146

CIRCLE NO 106

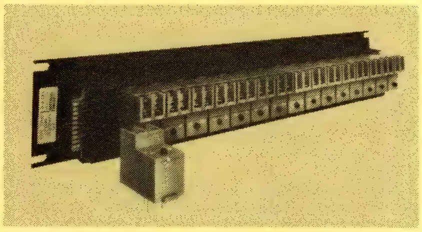
We'll bend over backwards to... **SPEED UP PRODUCTION OF YOUR COMPONENT LEAD BENDING OPERATIONS.**
MODELS N-300 & N-400



1. ***MEASURES EXACT BEND SPACING***
2. ***STRAIN RELIEF CLAMPING***
3. ***MAKES PRECISION BENDS FOR EASY INSTALLATION***

HARWIL ***1548 17th St. Santa Monica, Ca. 90404*** ***(213) 829-2310***

CIRCLE NO 107

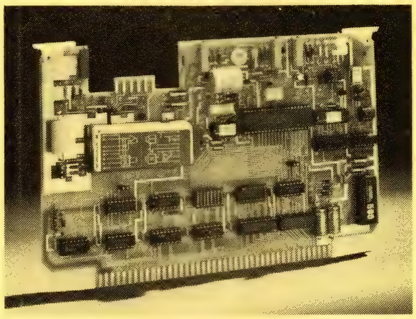


SOLID STATE I/O MODULES AC & DC

Teledyne's 673 series of I/O converter modules are for use in programmable controllers, machine tool controls, computerized process controllers, etc. Solid State technology with unique packaging concept provides reliable, noise-free I/O interface switching circuits between computer and loads. Send for complete info on these modules and free copy of Teledyne's I/O interface handbook. **Teledyne Relays,** 12525 Daphne Ave., Hawthorne, CA 90250 (213) 777-0077.

CIRCLE NO 108

MIKUL 6079 TEMPERATURE CONTROL BOARD



TEMPERATURE CONTROL BOARD digitizes thermocouple input using high CMR isolation amp and option of 16, 14 or 12-bit A/D converter. Cold-junction compensation and open T/C indication are provided. Also on-board is a D/A conv. (optional 10, 9 or 8-bit) with 10V output. Uses 5V supply with DC-DC conv. Fits Motorola EXORciser~ bus. Price $679 with 12-bit ADC/8-bit DAC.

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(419) 666-8144

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Electronic Devices, Inc.'s new, unique integral heat sink design provides superior heat dissipation for lower junction operating temperature and therefore greater reliability. Thermal impedance, junction-to-case, is as low as 1° C/W, which is significantly better than most metal case designs. Arc-over paths are also increased. The "KC" design ratings: 35 Amperes, to 1,000 PRV, to 400 Amp. Surge.

For FREE SAMPLES and information, write **Electronic Devices, Inc.,** 21 Gray Oaks Avenue, Yonkers, New York, N.Y. 10710.

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OR CALL
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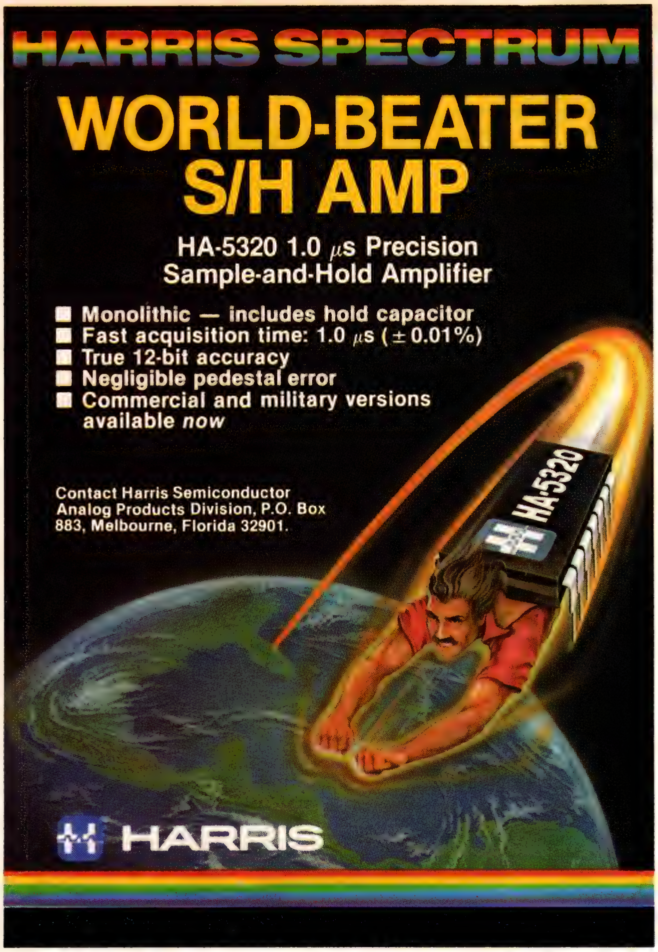
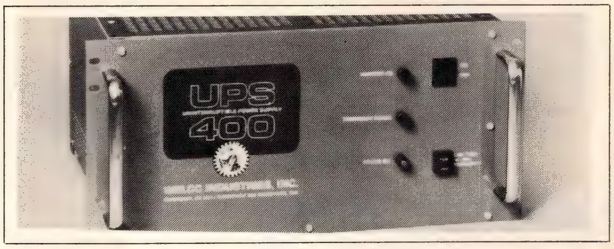


CIRCLE NO 80

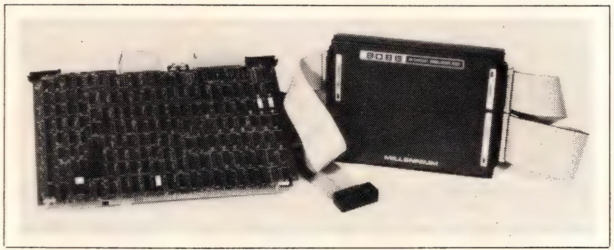
Instrumentation & Power Sources



UPS. Producing reliable transient-free power to protect equipment from noisy or unreliable power-source malfunctions and breakdowns, this uninterruptible unit permits equipment operation despite glitches, spikes, brownouts or power outages. It fits in a 19-in. rack and requires no line conditioners or dedicated lines. Clean, transient-free sine-wave output provides 400 VA max continuously, output voltage is maintained within ±3% and output frequency varies 1%. Output wave distortion is <5%; no single harmonic exceeds 3% of its fundamental. The unit's output inverter withstands 150% overload, is protected against overloads and short circuits and is rated for 400W continuous at unity power factor. $1360. **Welco Industries Inc,** 9027 Shell Rd, Cincinnati, OH 45236. Phone (513) 891-6600.

Circle No 297

Instrumentation & Power Sources



8086 EMULATOR. For use with the 9516 integration and debugging station, this unit provides transparent emulation and supports minimum and maximum as well as queue operations within the 8086 providing the user full control over breakpoint and trace at both input and output. It incurs minimal delays on user lines because it does not obstruct any memory, I/O or other processor resources. Key features include trace controls and hardware and software breakpoints on both bus activity (queue input) and instruction execution (queue output), externally reconstructed execution queue, and support of request and grant lines and Hold/Hold Acknowledge functions. The device can mask and monitor all the 8086's pins. $2895. **Gould Inc,** Millennium Instruments Div, 4600 Old Ironsides Dr, Santa Clara, CA 95050. Phone (408) 988-6800.

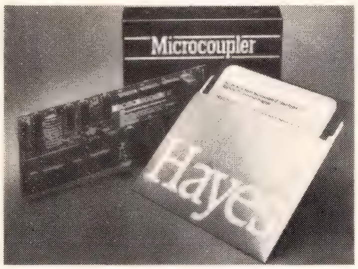
Circle No 296

CIRCLE NO 81

Software

SCREEN EDITOR. Available for all versions of the UCSD PASCAL system, the Advanced System Editor (ASE) provides user-definable function keys (macros) for use on many hardware systems, including the IBM Personal Computer and Apple II. The package edits very large files, provides menu-based file selection, edits a new file while still within another and requires simplified keystroke sequences for the most commonly used functions. Cursor-positioning commands permit such functions as moving word by word, moving backwards by one screen, moving to the beginning or end of a line, deleting by words or returning to the Home position. You also can recall search or replacement strings or move portions of the text horizontally (opening or closing space). Change logging maintains a dated log of each editing session. The software furnishes a separate configuration program that permits redefinition of commands or capabilities. Object- and source-code versions are available. $175. **Volition Systems,** Box 1236, Del Mar, CA 92014. Phone (714) 457-3865.

Circle No 268



COMM SOFTWARE. Designed for use with the manufacturer's Micromodem II and the Apple II µC, the Terminal Program originates and answers calls; creates, lists, sends and receives files; and manages communications parameters as directed by commands selected from a menu or list of options. Compatible with three Apple operating systems (DOS 3.3, PASCAL and CP/M), it provides three file-transfer protocols: Stop/Start, Send Lines and Verification. The package supports six disk drives, several printer-interface cards, 40- and 80-column screens and lower-case characters. It also stores three phone numbers and one prefix. $79 (disk and backup disk without Micromodem II); $399 with Micromodem II. **Hayes Microcomputer Products Inc,** 5835 Peachtree Corners East, Norcross, GA 30092. Phone (404) 449-8791.

Circle No 269

DATA PROTECTION. Using the US Bureau of Standard DES algorithm, Datalok provides data protection for the Apple II computer. Its hardware portion includes a WD2001 DES chip on a board configured for the Apple Bus; its software encrypts and decrypts any file created under Apple DOS and can also lock and unlock an entire disk. The system requires an Apple II with 48k of RAM, one disk drive, Apple DOS 3.2 or 3.3 and Apple Soft BASIC. $349. **Atlantis Computers,** 31-14 Broadway, Astoria, NY 11106. Phone (212) 728-6700.

Circle No 270

EPROM SIMULATOR. ESM interfaces with a wide variety of commonly used EPROM-simulating systems, including the Avocet PSB-100. I/O routines in source code allow you to modify or add your own EPROM-simulator drivers. A control block (used to identify the type of EPROM to be simulated) eliminates the need for length calculations and provides adaptability to future EPROMs. The target memory is referenced directly without address-offset calculations and can be one of several EPROMs in the target system. Distributed on 8-in. single-sided, single-density diskettes, the program runs under CP/M Version 2.0 or above and requires at least 24k of RAM. A HexROM utility is also included for hex-file conversion. $195. **Dantek Software Inc,** 4550 Schoolhouse Rd, Batavia, OH 45103. Phone (513) 752-1921.

Circle No 271

PASCAL TUTORIAL. Consisting of two sets of tutorial programs on diskette, SofTeach helps you learn to use and understand UCSD PASCAL. The first program utilizes the "revealed-choice" technique to question you about various aspects of the UCSD PASCAL language; the second tests your ability to implement this new knowledge by writing procedures and functions. Also included is *The UCSD PASCAL Handbook.* $125. **SofTech Microsystems,** 9494 Black Mountain Rd, San Diego, CA 92126. Phone (714) 578-6105. TWX 910-335-1594.

Circle No 272

VISICALC CONVERTER. Capable of converting any text file to a VisiCalc (DIF) file, LoadCalc provides a screen menu and commands similar to those of VisiCalc. Fractions are interpreted and converted to decimals; the software allows you to edit and select data for conversion by row and column. Each field is analyzed and saved as either a label or a value in a DIF file; no programming is required. $95 for Apple II+; IBM version also available. **Cypher,** 121 Second St, San Francisco, CA 94105. Phone (415) 974-5297.

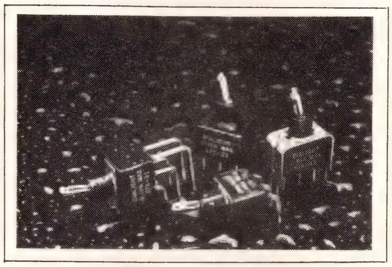
Circle No 273

FIBER-OPTIC MODEM. The FOM-1232, an ac-power, all-aluminum-enclosed turnkey system, includes an asynchronous link that operates at any data rate from dc to 56,000 bps and meets all RS-232C interface requirements for Type D data-communications equipment. Its transmitter uses a microlensed 820-nm LED emitter that couples 20 μW into a 200-μm-core step-index fiber. Its PIN-diode detector provides 10-nW sensitivity for a worst-case bit-error rate of 10^{-9}. More than 4000m can be traversed with either 7-dB/km, 200-μm step-index or 5-dB/km, 50-μm graded-index fibers. Duplex operation requires a duplex cable or two single-channel cables. The unit provides full handshaking capability, and four threaded inserts on the bottom surface permit permanent mounting. Electrical connections occur via a 25-pin D connector; standard optical connectors are SMA type. $200 (100). **Manage Inc,** Box 175, Chicopee, MA 01014. Phone (413) 592-3834.

Circle No 259

HYBRID AMPLIFIERS. Housed in TO-8 packages, Models 501, 502 and 503 of the GPA500 Series are self contained and span a 500-MHz to 1-GHz bandwidth. They feature noise figures of 3 dB, output power to 100 mW and gain to 15 dB. Models 510, 511 and 512 of the GPA510 Series supply a 500-MHz bandwidth, noise figures to 3.5 dB, output power to 100 mW and gain to 15 dB. External bias components are required. GPA500 Series units, $50.48; GPA510 Series devices, $25.23 (100). **TRW/Semiconductors,** 14520 Aviation Blvd, Lawndale, CA 90260. Phone (213) 679-4561. TWX 910-325-6206.

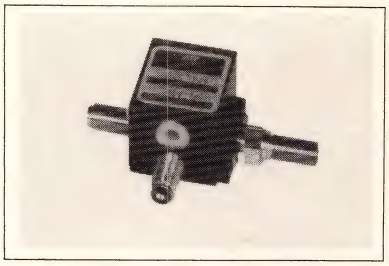
Circle No 260



TOGGLE SWITCHES. Series 578 sealed switches come in spdt and dpdt versions and feature a variety of epoxy-sealed terminal types: pc (right-angle mount with terminals bent at 90° or with 0.250-in.-long terminals) and wire - wrapping (1.062× 0.250 in.). Units also provide a choice of contact ratings to accommodate standard, low and combination standard/low current levels. Gold-plated contacts are available for current levels of 0.4VA max at 20V ac or dc; optional gold-over-silver contacts serve standard (1A at 120V ac/28V dc) and combination standard/low-level currents. $1.61 (1000). Delivery, 3 to 4 wks ARO. **Dialight,** 203 Harrison Pl, Brooklyn, NY 11237. Phone (212) 497-7600.

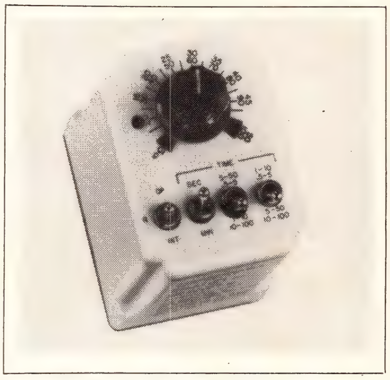
Circle No 261

FIBER-OPTIC SWITCH. Similar to an spdt electromechanical unit, the SW-92 specs response time of 3 msec and 2-dB attenuation. Switching current equals 300 mA at 24V dc. The



device comprises two solenoids, a moving mirror and an optical coupling system. Also available is a packaged control circuit operated by a panel-mounted switch. **Frequency Control Products Inc,** 61-20 Woodside Ave, Woodside, NY 11377. Phone (212) 458-5811.

Circle No 262



TIME-DELAY RELAYS. CW Series units program both timing function and delay time using four toggle switches and a knob on top of its case: The switches select timing function, timing mode (seconds or minutes) and timing range; the knob sets delay-time value, ranging from 0.5 to 5, 1 to 10, 5 to 50 and 10 to 100. Standard voltages are 24, 120 and 240V ac (50/60 Hz) and 12, 24, 48 and 110V dc. Power consumption specs at <3 VA for ac units and <3W for dc relays. Tolerance ranges from +0/−20% min to +10/−0% max, but not less than ±16 msec for ac models and ±10 msec for dc units. Repeatability equals ±0.5% max for dc models, and Δt is ±5% for the entire series. The relays offer 2 Form C (dpdt) contacts rated for 10A at 120 or

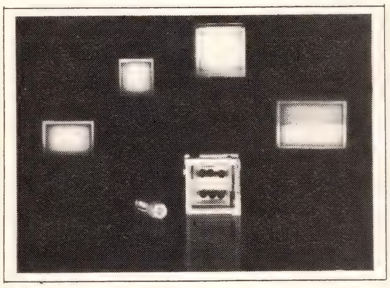
Components & Packaging

240V ac or 10A at 30V dc. An LED indicator lights when a unit's coil is energized. $80.33 (25). Delivery, 6 to 8 wks ARO. **Potter & Brumfield Div AMF Inc,** 200 Richland Creek Dr, Princeton, IN 47671. Phone (812) 386-2273.

Circle No 263

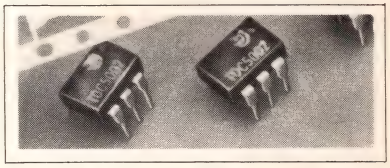
POWER AMPLIFIERS. Operating at 470 to 860 MHz, ATV 5000 Series units deliver as much as 8W output power at the 1-dB gain-compression point. They provide matched 50Ω input and operate from one 26 to 28V supply. The ATV 5020 version is an internally biased Class A unit with power gain of 7.5 dB min and delivers 25W output power at 1 dB gain compression. The ATV 5080, a Class AB part, specs power gain of 6 dB and delivers 80W at 1-dB gain compression. Its case temperature can span −20 to +70°C. ATV 5020, $1200; ATV 5080, $1300. Delivery, 4 to 6 wks ARO. **TRW/Semiconductors,** 14520 Aviation Blvd, Lawndale, CA 90260. Phone (213) 679-4561.

Circle No 264



LED PUSHBUTTONS. A3S Series subminiature units feature easy-to-replace 4-chip LED lamps; standard-sized A3P Series units incorporate multiple LEDs in an advanced lamp-circuit design integrating a screened-on limiting resistor. Both versions utilize an enhanced back-projected screen design and provide a wide choice of solid and bicolor patterns. Silver, gold-alloy and solid-state contact types come with solder or No 110 quick-connect combination terminals. $5.10 to $12.94 (1000). **Omron Electronics Inc,** Control Components Div, 650 Woodfield, Schaumburg, IL 60195. Phone (312) 843-7900.

Circle No 265



SOLID-STATE RELAY. Rated to ½A and 60V ac pk, the TOC 5002 incorporates zero-voltage switching and optical isolation of 2500V ac min. Housed in a 6-pin DIP, it requires <2-mA turn-on current. OFF-state leakage is <500 mA. UL recognized, the device meets FCC and VDE RFI standards. $3.10 to $5.40 (1000), depending on voltage. **Theta J Corp,** 208 W Cummings Park, Woburn, MA 01801. Phone (617) 935-7600.

Circle No 266

PRESS-FIT CONNECTOR. The D-subminiature C-Press comes in pin- and socket-board-mounting versions with 9, 15, 25 or 37 positions. Constructed from copper alloy No 725, its contacts can be selectively plated. The unit's insulator is natural-white glass-reinforced thermoplastic, and operating temperature spans −55 to +105°C. The socket design features a closed-entry design to avoid misalignment when mating. Threaded bushings (No 4-40 and No 6-32 UNC) and a quick-latch system are available. Pin version, $3.15; socket unit, $3.47 (1000). **Winchester Electronics,** Oakville, CT 06779. Phone (203) 755-5000.

Circle No 267

5½/6½-digit full-function benchtop DMM incorporates talker/listener IEEE-488 bus

Containing complete talker/listener IEEE-488 interfacing, Model 7150 5½/6½-digit automatic-calibration DMM is designed to take advantage of low-cost intelligent bus controllers. It performs A/D conversion using the pulse-width method, providing precision measurements to 0.01% basic accuracy. Short integrations (to 6 msec) are possible when speed is essential, along with longer times for interference rejection: you can choose five different averaging periods.

Averaging adds a digit

Designed for benchtop use, the meter furnishes a 5½-digit basic reading that extends to 6½ digits via digital averaging over 10 measurement cycles. Because updates are performed after each reading through use of a walking average, a full 6½-digit reading update occurs every 400 msec. Bus users can shorten scale length to 3½ digits, however, to increase reading speed to about 25 readings/sec max (depending on the controller used); range changes vary from 20 to 100 msec.

Measurements include dc voltage from 0.1 μV to 1000V, true-rms ac voltage from 10 μV to 750V, dc and ac current from 1 μA to 2A, resistance from 10 mΩ to 20 MΩ, and diode test at 100 μA. Accuracy for dc voltage specs at 0.002% for 24 hrs and 0.01% over 2 yrs. For ac voltage, the corresponding figures (mid-range) are 0.1% and 0.16%. Bandwidth spans 10 Hz to 300 kHz. In normal use, the instrument is autoranging, but you can disable this feature.

Readings appear on a full-sized custom LCD, backlit for enhanced clarity. Prompts above the numerals indicate mode of use, and a Freeze facility permits holding any reading. (In this mode, though, the meter continues to monitor input, flashing the display if an overload occurs.)

Extending scale length to 6½ digits via digital averaging, *Model 7150 DMM incorporates full talker/listener IEEE-488 interfacing as a standard capability.*

IEEE-bus oriented

Concentrating on the measurement function, the standard instrument contains full talker/listener IEEE-488 interfacing—a design philosophy that takes advantage of the many low-cost intelligent bus controllers now available. Independent calibration of any range occurs over the bus with no need to remove covers; coefficients are held in nonvolatile EAROM.

Because of the ADC's linearity, you must enter only high and low points, from which the characteristic is adjusted for slope and intercept. Before calibration, you must insert a jack plug into the back panel—a simple protection mechanism against accidental or unauthorized changes.

In addition to autocalibration, the instrument provides an automatic and independent null on resistance and dc voltage and current. £750. Delivery, 4 to 6 wks ARO.

Solartron Ltd, Victoria Rd, Farnborough, Hants GU14 7PW, UK. Phone (0252) 544433.

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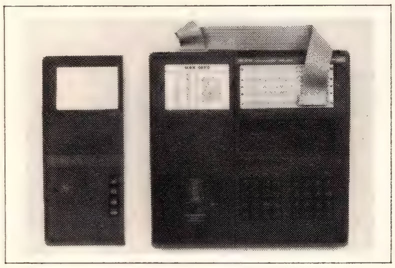
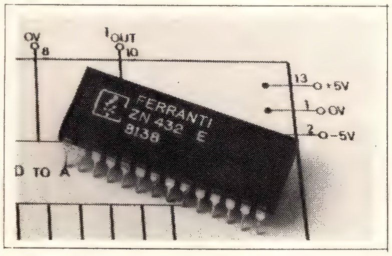


DEVELOPMENT MODULE. The PM4337 personality module configures its manufacturer's PM4300 microcomputer instructor for 8400 single-chip-μC program development. Using the device's MAB8400Q bondout version as a target processor makes dc and ac behavior virtually identical (the only difference is the extra capacitance of the pins accessed through the emulation cable). All I/O ports on the emulation probe have push/pull output with pull-up, except for the device's I²C bus (serial I/O), which has an open-drain output. Facilities include hardware breakpoint, single and automatic stepping, manual interrupt, port and data-memory examination and a disassembler. The unit contains an integral programmer for 2716- and 2732-type EPROMs. **N V Philips' Gloeilampenfabrieken,** Elcoma Div, Box 523, 5600 AM, Eindhoven, The Netherlands. Phone (040) 723142.

INQUIRE DIRECT



10-BIT ADC. Model ZN432E plastic-packaged monolithic A/D converter features guaranteed conversion time of 20 μsec with no missing codes. Utilizing the successive-approximation technique, it includes an on-chip 2.5V reference. Fabricated in the CDI bipolar process and operating over 0 to 70°C, the 28-pin device is TTL/CMOS compatible and requires ±5V supplies. £8.71 (100). **Ferranti Electronics Ltd,** Fields New Rd, Chadderton, Oldham, Lancs OL9 8NP, UK. Phone (061) 624-0515.

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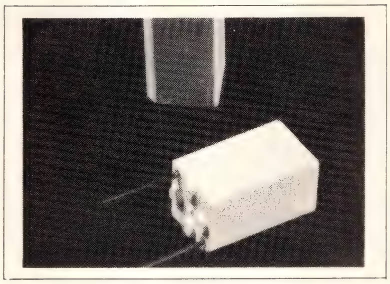

FILM CAPACITORS. Miniature PHE425 polypropylene capacitors utilize ultrathin 4-μm metallized film. They come in finished sizes as small as 6.3 mm square, suiting them for high-density pc-board applications. Maximum heights are similarly low—11 or 13 mm—matching RM5 and RM6 ferrite-core requirements. Available in values from 1.5 to 135 nF, the devices come in ±1, +2 or ±5% tolerances, with insulation resistance better than 200,000 MΩ at 20°C and 10V dc. Standard voltage ratings equal 63, 100 and 200V dc. Enclosed in an epoxy-filled self-extinguishing polypropylene box, the units have connecting leads on 0.1-in. centers. **RIFA AB,** Box 2, S-16300 Spånga-Stockholm, Sweden. Phone (08) 752 2500.

INQUIRE DIRECT

64k-BYTE NONVOLATILE RAM. A lithium battery provides 10-yr data-retention life for the NVR64 64k×8 RAM module. Featuring 150-nsec cycle time and an unlimited number of read/write cycles, the 4×2×1-in. unit provides internal buffering that allows you to plug it directly onto a μP bus. Interfacing signals are the same as those used by standard static RAM; connection occurs via a standard DIN-type indirect connector compatible with a pc board, backplane or IDCs. £375. Delivery, 3 to 4 wks ARO. **Greenwich Instruments Ltd,** 22 Bardsley Lane, Greenwich, London SE10 9RF, UK. Phone (01) 853 0868.

INQUIRE DIRECT

WAVEFORM RECORDER. Firmware routines for rise-time, slope and rms analysis come standard in the DL1080 programmable waveform recorder, reducing the need for data transfer to external processors. The firmware package adds 20 functions and provides remote access to processing functions over an IEEE-488-bus interface. An automatic sequence generator allows initiation of complete routines via one keystroke or bus command. £6895. **Data Laboratories Ltd,** 28 Wates Way, Mitcham, Surrey CR4 4HR, UK. Phone (01) 640 5321.

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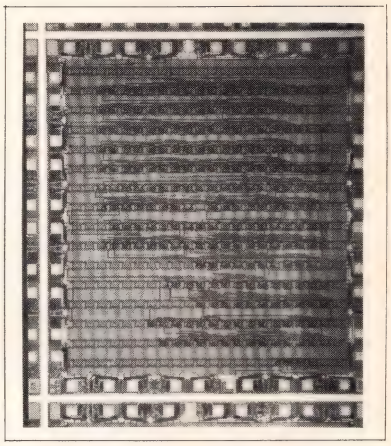

CMOS GATE ARRAY. First in a family, the PC0700 contains 700 gates and is fabricated with LOCMOS technology. The manufacturer claims a turnaround time of 10 wks from receipt of your logic circuit to shipment of

samples, thanks to network-description, logic-simulation, automatic-wiring, maskmaking and test-pattern verification/test CAD tools. Depending on supply voltage, typical delay time (for fanout of two) ranges from 1.7 to 7 nsec; toggle frequency measures 12 to 30 MHz. Every device in the family will have pull-up/down resistors and I/O pads; the PCO700 incorporates 34 and 38 of each, respectively. Versions with 250, 500 and 1000 gates will be available by the end of 1982. **NV Philips' Gloeilampenfabrieken,** Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 79 1111.

INQUIRE DIRECT

PHONE IC. Replacing rotary dialers in standard telephone handsets, the 18- or 24-pin CMOS M760 loop-disconnect dialer is mask programmable to meet various countries' timing requirements. Powered from the line, it connects directly to a single-contact keypad, generating current-pulse streams that simulate mechanical dialers. Features include 24-digit last-number redial, pin-selectable long-distance call or redial inhibit and an input to block the pulse generator for pay-phone applications. Keyboard inputs are fully static, and outputs are provided to mute the speech circuit during signaling. A 455-kHz ceramic resonator determines frequency. **SGS Ates SpA,** Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551.

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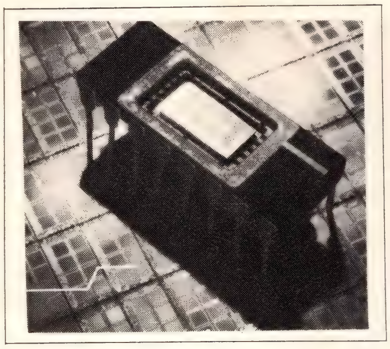
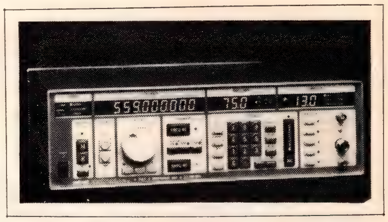


64k RAM. Pin compatible with industry-standard dynamic RAMs, Model IMS2600 provides an additional Nibble mode, allowing high-speed serial access of as many as four data bits and thus providing the equivalent of 4-way on-chip interleaving. Packaged in a standard 16-pin DIP, it comes in 100- and 120-nsec versions, using 4-msec/256-cycle refresh. $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh provides an on-chip mechanism that's upwardly compatible with that of 256k RAMs because pin 1 is left unconnected. Cycle times for the two versions equal 160 and 190 nsec; power consumption specs at 220 and 360 mW (17 mW standby). Output can be held valid indefinitely by holding $\overline{\text{CAS}}$ LOW. 100- and 120-nsec versions, £17.34 and £13.39 (100), respectively. Delivery, 6 to 8 wks ARO. **Inmos Ltd,** Whitefriars, Lewins Mead, Bristol BS1 2NP, UK. Phone (0272) 290861.

INQUIRE DIRECT

RF SIGNAL GENERATOR. The µP-controlled Model 740A covers 100 kHz to 1120 MHz, derived from a crystal pilot driving a 10-Hz step synthesizer. A doubler option serves 560 to 1120 MHz. Output level spans −128 to +13 dBm throughout the range, with attenuator preci-



sion of ±1.5 dB to −100 dBm. Modulation and output stages provide amplitude-, phase- and optional pulse-modulation facilities. Use of the Execute command allows preparation and checking of new operating configurations without interrupting a currently running program and also permits switching between configurations without transients. 47,000 FF. Delivery, 4 months ARO. **Giga Instrumentation,** 37 Avenue de la Marne, 92120 Montrouge, France. Phone (1) 657 60 26.

INQUIRE DIRECT

Z80 EUROCARD. Model IMSCPU2 processor card works with its manufacturer's IMS industrial microcomputer system of 100×160-mm Eurocard modules. Operating at 4- or 2-MHz clock rates or from an external clock, it provides on-card sockets that accept 32k bytes of PROM, EPROM or compatible RAM; you can also implement a DMA scheme. Memory addressing is selectable, and the unit incorporates a watchdog timer, one 8-bit input port and one 8-bit output port. Systems can be prototyped on the Supermodest development system, comprising a rack, Z80-based CPU, 32k of RAM, diskette controller, parallel and serial interfaces, power supply and twin 5¼-in. floppy-disk drives operating under CP/M (10,000 to 15,000 Guilders). **N V Philips' Gloeilampenfabrieken,** Elcoma Div, Bldg BA, 5600 MD, Eindhoven, The Netherlands. Phone (040) 723142.

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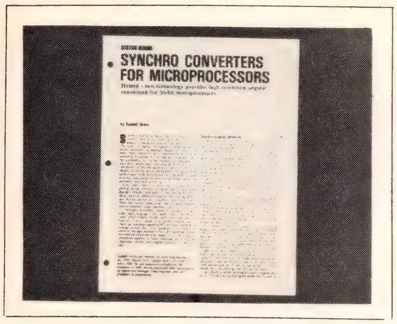
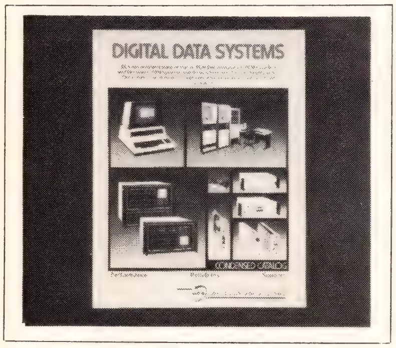


Synchro converters for μPs

This 4-pg reprint discusses the interfacing of a line of hybrid synchro-converter ICs with 8- and 16-bit μPs. Diagrams illustrate interfacing via an asynchronous bus and interface timing for a digital-to-synchro converter interfaced with a 16-bit μP. In addition, the article covers typical synchro-converter applications. **Natel Engineering Co Inc,** 8954 Mason Ave, Chatsworth, CA 91311.

Circle No 298



Data-acquisition facts

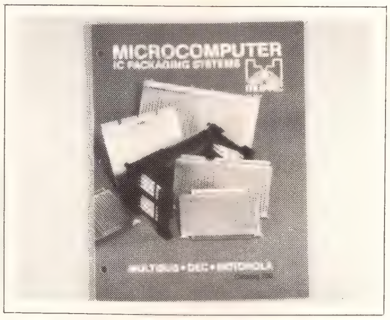
Featuring Series 5000 stored-program PCM decommutation systems, this 8-pg catalog details their μP-controlled operation and standard peripherals. It also examines a line of PCM bit synchronizers ranging from small plug-ins to the computer-controlled, tunable Model 4781. Finally, the booklet describes the 5600 tape-formatting system via block diagrams. **Data-Control Systems,** Commerce Dr, Danbury, CT 06810.

Circle No 299

Ultrasonic flaw detection

This 10-pg booklet describes three configurations of M90 Reflectoscope Series modular ultrasonic flaw detectors, introducing two units: the M91 and M91-C. General descriptions of each instrument are followed by technical data and module photos. The booklet highlights capabilities previously unavailable in a compact flaw detector, according to the manufacturer, and describes optional features such as DAG or DAC modes of distance/amplitude compensation and a curve-matching computer. **Automation Industries Inc,** Sperry Products Div, Shelter Rock Rd, Danbury, CT 06810.

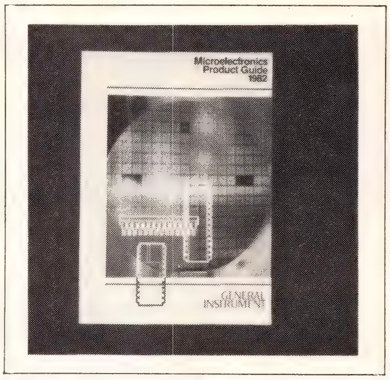
Circle No 300



IC-packaging options

Showcasing a family of microcomputer IC-packaging systems, this 20-pg catalog highlights the line's design features: V_{CC} and GND I/O, noise suppression, closely spaced ICs, flexible I/O layout and wire-wrapping pins. One section discusses features and applications of Multibus-compatible products, and another examines DEC-compatible units. Dimensional drawings, photos and spec charts illustrate packaging systems, and sections on materials, finishes and accessories conclude the booklet. **Mupac Corp,** 10 Mupac Dr, Brockton, MA 02401.

Circle No 301



Microelectronics: processes and products

This literature packet includes seven data sheets, a 24-pg catalog and a booklet that summarizes the technology used in the company's microcircuits. The catalog provides specs for a line of ROMs, including speech units; speech processors; keyboards; μCs; encoders; character generators; EEPROMs/EPROMs; and audio, video and tuning products. The pamphlet discusses photomask-set preparation, wafer processing and device assembly and terminates with a glossary of microelectronics terms. **General Instrument Corp,** Microelectronics Div, 600 W John St, Hicksville, NY 11802.

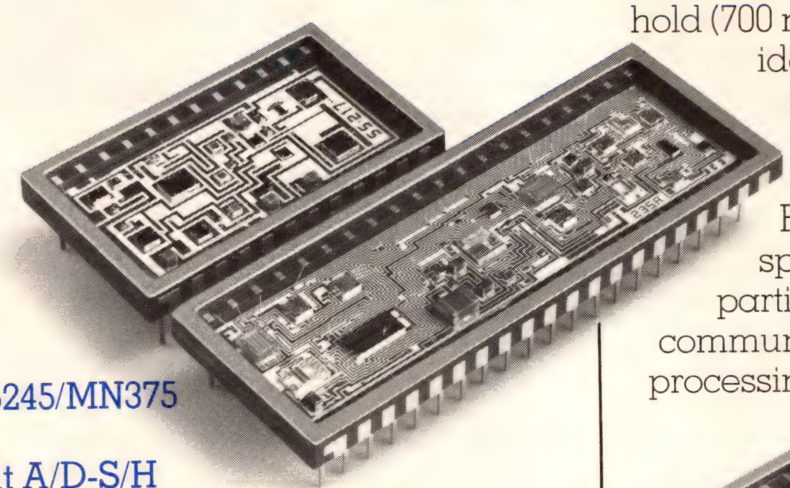
Circle No 302

Regulating voltage

Featuring 11 models of 3-terminal voltage regulators with output voltages of 5 to 24V dc, this 28-pg catalog provides electrical characteristics and temperature-derating curves. It illustrates device test circuits and explains how to increase output current or voltage using a few external components. Highlighted are the units' ability to deliver as much as 1A at their rated output voltage. **Panasonic Industrial Co,** Electronic Components Div, 1 Panasonic Way, Secaucus, NJ 07094.

Circle No 303

WIDEBAND

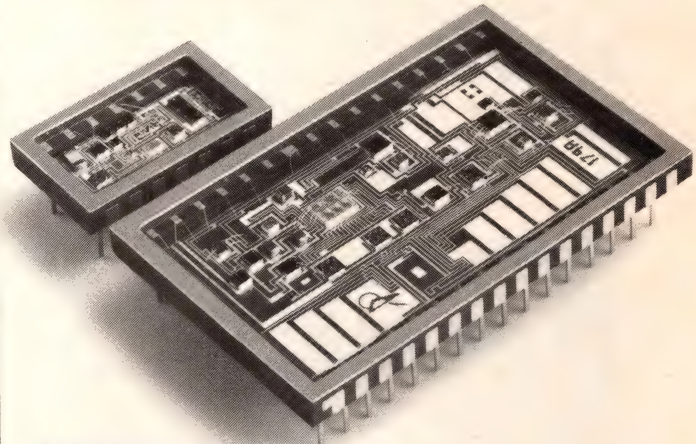


MN5245/MN375

12 Bit A/D-S/H
Minimum Thruput: 500 kHz
System Bandwidth: 775 kHz
No Missing Codes Guaranteed
Optional MIL-STD-883 Screening

We offer the broadest line of analog-to-digital converter/sample-hold combinations. These highly optimized systems increase your ability to accurately sample broader bandwidth analog signals. From our selection of highly accurate systems, pick the perfect pair for your application: very-high-speed, high-speed, or low-cost.

For your highest speed requirements, our MN5245 900 nsec 12 Bit A/D combined with our MN375 sample and hold (700 nsec acquisition time) is ideal. It will accurately digitize signals with frequencies up to 775 kHz, a vast improvement over the use of *any* single 12 Bit A/D converter. Its very high speed makes this combination particularly useful in digital communications, digital signal processing, and spectrum analysis.



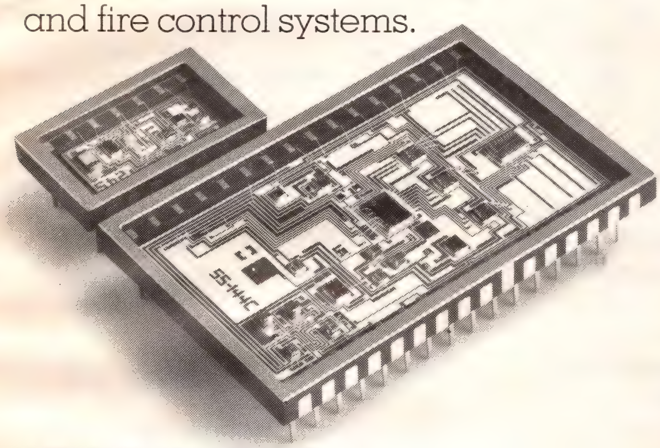
MN5240/MN346

12 Bit A/D-S/H
Minimum Thruput: 133 kHz
System Bandwidth: 190 kHz
No Missing Codes Guaranteed
Optional MIL-STD-883 Screening

For an excellent performance/cost balance, combine our MN5240 5 µsec

DIGITIZERS

12 Bit A/D converter with the MN346 sample and hold (2 μsec acquisition time). You'll accurately capture signals having frequencies up to 190 kHz. This pair is especially suited to high-speed data acquisition, avionics, guidance and fire control systems.



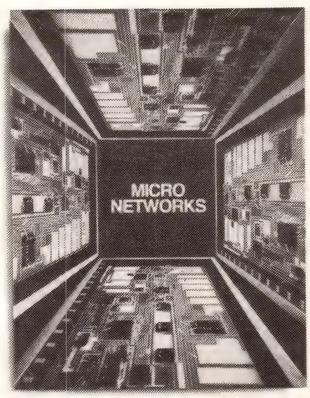
MNADC80/MN340

12 Bit A/D-S/H
Minimum Thruput: 33 kHz
System Bandwidth: 190 kHz
No Missing Codes Guaranteed
Optional MIL-STD-883 Screening

And if your application is particularly cost-sensitive, our 25 μsec ADC80 coupled with our new MN340 sample and hold (4 μsec acquisition time) is the perfect choice. Use it for process control, medical instrumentation, and general purpose data acquisition.

We're a veritable supermarket for military and industry-proven digitizing components. For industrial and military applications, whether state-of-the-art or cost-sensitive, you won't find a more accurate or efficient line of data conversion products.

Send for your data sheets on any of these perfect couples. For fast action or for your copy of our 250-page catalog, call John Munn (617) 852-5400, or write to:



Micro Networks Company
324 Clark Street
Worcester, MA 01606

Micro Networks
Advancing Data Conversion Technology

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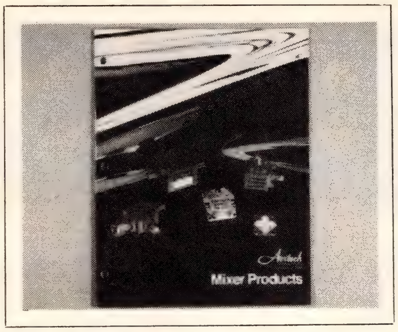
CIRCLE NO 85



Data details 1- to 18-GHz mixer products

Featuring a line of mixers, mixer preamps and frequency doublers, this 22-pg catalog defines such terms as conversion loss, isolation, dynamic range and noise figure. Schematics illustrate a discussion of such applications as down and up conversion; phase detection; and amplitude, pulse and biphase modulation. Specs characterize various models by frequency, RF-IF gain, isolation and flatness, and graphs plot typical performance factors. **Aertech Industries,** 825 Stewart Dr, Sunnyvale, CA 94086.

Circle No 304

Selecting S-100-bus products

Listing more than 450 S-100-bus-compatible board-level products from more than 65 manufacturers, this guide covers 23 μC-product categories, such as single-board computers, peripheral controllers and video boards. Published semiannually, it includes design and performance specs, prices, and delivery and availability data. For each product discussed, it also provides date first manufactured and manufacturer's sales offices. $25, prepaid; $35, outside continental US. Additional copies, $9.95 ea. **Ironoak Co,** 3239 Caminito Ameca, La Jolla, CA 92037.

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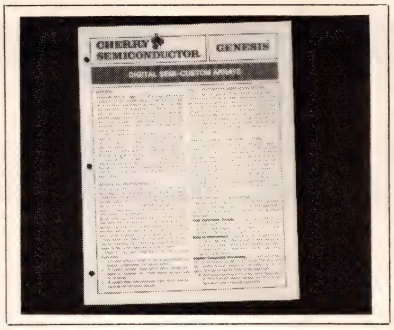

Designing with digital semicustom arrays

Describing the advantages of I²L technology, this packet comprising data sheets and a 6-pg brochure reviews basic layout rules for three digital-chip types: the Genesis 1200, 1300 and 1400. Charts and diagrams illustrate the basic I²L gates, I/O interfaces and components. A chart of the company's circuit line provides specs for seven linear circuits and three digital ones. Features of I²L technology discussed include high functional density, ease of connection, bipolar-compatible processing and wide operating-temperature range. **Cherry Semiconductor Corp,** 2000 S Country Trail, East Greenwich, RI 02818.

Circle No 305

Geometry modeling for advanced CAD/CAM

This 6-pg booklet discusses the Euclid CAD/CAM design package, which runs on VAX computers. A section on applications outlines capabilities for drafting, numerical-control programming, kinetic analysis, drawing schematics and finite-element modeling. The text also highlights the system's ability to work directly on 3-dimensional solids and such features as hidden-line removal, mass-property analysis, sectioning and fusing. **Digital Equipment Corp,** 200 Forest St, Marlboro, MA 01752.

Circle No 306

Testing at low temperatures

Presenting techniques for probing and testing semiconductor chips, wafers and hybrid circuits, this app note describes methods of preventing the frost and moisture condensation that normally occur during tests at low temperatures. It explains how ThermoChuck Systems utilize temperature-controlled precision platforms (chucks) that can be used on the stage of almost any microprober or microscope to test semiconductor devices, materials or specimens at controlled temperatures with an accuracy of ±1°C and repeatability to ±0.5°C. **Temptronic Corp,** 55 Chapel St, Newton, MA 02158.

Circle No 307

Selecting switch products

Detailing a line that includes rotary-switch assemblies and components, special-purpose switches, keypads, relays and solenoids, this 28-pg catalog discusses sizes, mounting instructions, operating life, materials and performance characteristics. Schematics and dimensional drawings illustrate the products. **Oak Switch Systems Inc,** Box 517, Crystal Lake, IL 60014.

Circle No 308

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Application forms and further details are available from:
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Circle No. 5000 (on page 212 of **EDN**)

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Circle No. 5001 (on page 212 of **EDN**)

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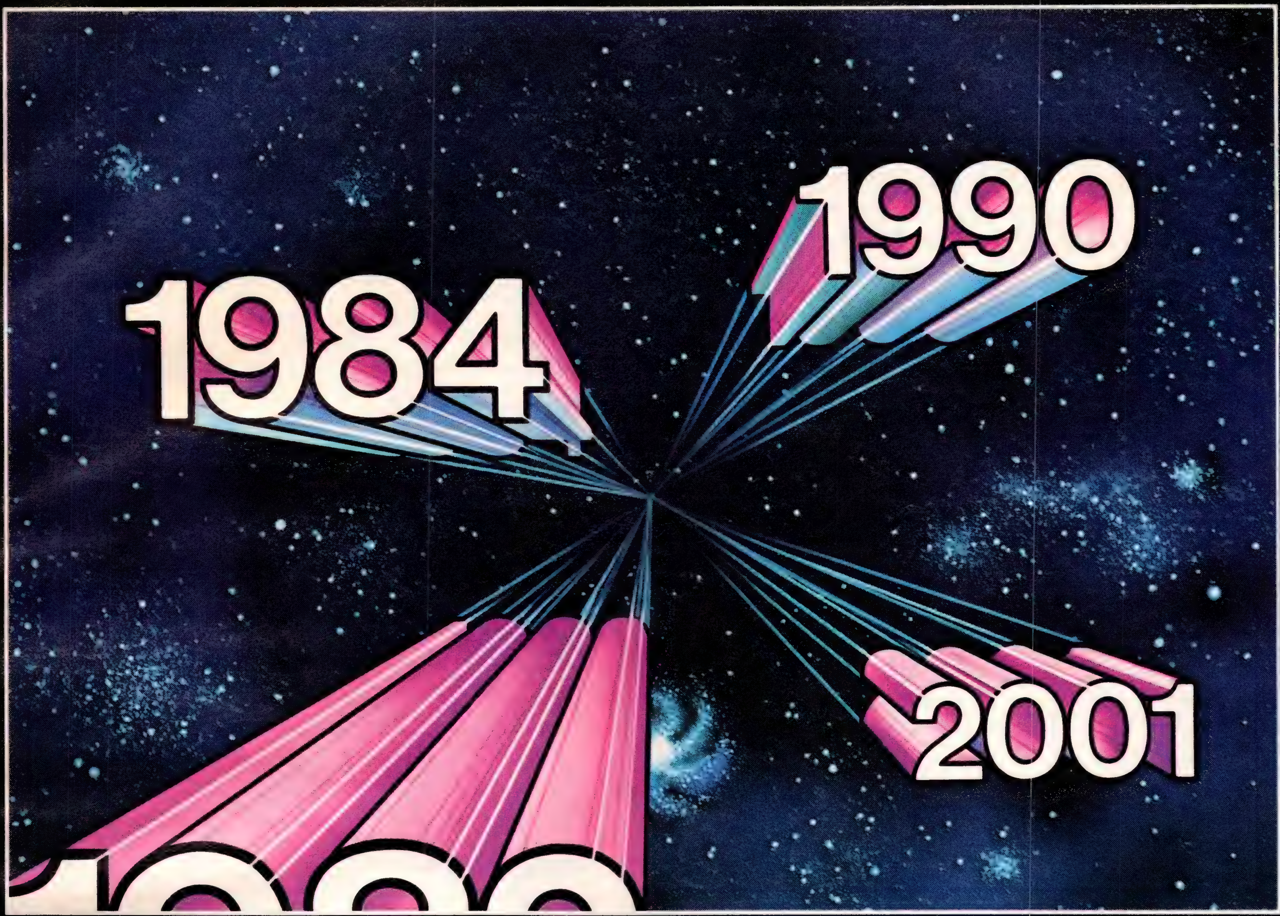

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Looking Ahead: Trends and Forecasts

Videotex technology gains momentum

Recent developments in US and European videotex markets will have major repercussions on the fledgling industry and illustrate the technology's growing viability. In the most significant of these, IBM will enter the US videotex arena with a private corporate system for sending and receiving text and graphics. The firm's Series/1 Videotex System (SVS/1), first introduced in Europe, has a 1-time license fee of $10,000 and can respond to 24 concurrent videotex calls, store as many as 350,000 frames of information and handle internal mail, budgets, sales and merchandising data, travel schedules, and bulletin-board services.

Requiring a minimum $56,000 to $200,000 expenditure for software and hardware, the Series/1-computer-based system will use standard phone lines to connect IBM Personal Computers, specially adapted TV monitors or low-cost videotex terminals. Utilizing a standard similar to that of the British Prestel system, it will be incompatible with AT&T's announced videotex standards (based on the Canadian Telidon system).

In other developments:

- Joining with NBC and CBS, RCA has adopted the North American Broadcast Teletext Specification (NABTS) for its proposed home-TV teletext service. The initial system will use dynamically redefined character sets and picture-description instructions (PDIs) to provide quality graphics.
- Credit Commercial de France, a major French bank, has installed a Teletel-based videotex system connecting its major corporate accounts with branch offices. The 24-hr *Videobanque* service utilizes Matra or TRT Minitel terminals similar to those employed in the French electronic Yellow Pages service and provides on-line access to statements and balances as well as electronic mail, check tracing, economic analysis, exchange rates and stock-exchange data. Nationwide access to the system will be available via local phone calls, distributed gateways and the Transpac X.25 national packet-switching net.
- Iris, a bilingual Telidon-based Canadian videotex system, will begin a 3-yr test starting this month in Montreal, Toronto and Calgary.
- Sony Corp will enter the videotex market, producing RGB monitors, decoders, keyboards and black-and-white and color printers that are compatible with various systems.

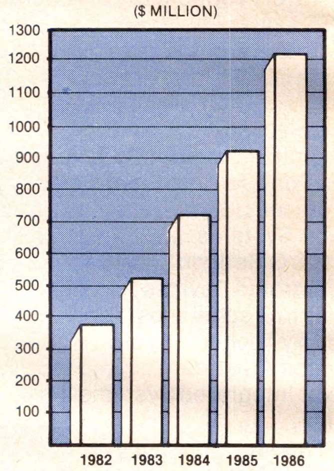
Data-converter market to grow to $1.2B in '86

The data-converter market is slated for massive expansion. Fueled by the pervasive shift toward digital techniques in all segments of electronic instrumentation, the market for A/D and D/A converters, S/H amplifiers and analog multiplexers will jump to $1.2 billion in 1986, rising at a 33% average annual rate from 1982's expected $377 million level, predicts Venture Development Corp (VDC), Wellesley, MA.

Nowhere is the trend toward digital techniques more apparent than in industrial measurement and control, as μP-based controllers rapidly supplant analog units, particularly in temperature-measurement applications. Other key digital application areas include robots, CAD/CAM systems and ATE.

Although the military market will exhibit somewhat less dramatic growth, VDC also foresees increased converter usage in radar, navigation and communications applications. Furthermore, medical applications, such as automatic blood analysis and digital imaging, will continue to be significantly large users of digital techniques.

A/D- AND D/A-CONVERTER, S/H-AMPLIFIER AND ANALOG-MULTIPLEXER SHIPMENTS



SOURCE: VENTURE DEVELOPMENT CORP

Consumer markets, however, could ultimately constitute the largest application area for A/D and D/A converters, VDC says. It forecasts heavy usage in appliances, games, environmental and energy control and perhaps digital photography.

Material for this page developed from *Electronic Business* magazine and other sources by Jesse Victor, Senior Staff Editor, and Joan Morrow, Assistant Editor.